Research Agenda
Of
A. Marzuki

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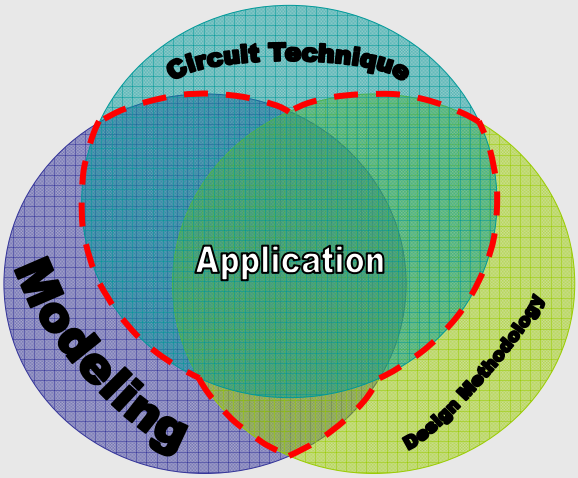
Integrated Circuit (IC)

CTDMM

Circuit Technique, Design Methodology and Modeling

Research Vision & Mission: To excel in circuit technique, design methodology and modeling in Analog, RF and Mixed-Signal IC. To employ knowledge and expertise from Universities and Industries.



Arjuna Marzuki obtained his B.Eng (Honours) from the department of Electronic and Electrical Engineering at the University of Sheffield in United Kingdom, MSc from Universiti Sains Malaysia and PhD from Universiti Malaysia Perlis. He has more than 10 years of experience as IC design engineer in Hewlett-Packard/Agilent Technologies, and IC Microsystem. Arjuna has to-date filed 4 international patents and published more than 20 technical papers. He is currently a lecturer with Electrical and Electronic School at Universiti Sains Malaysia and an associate research fellow with Collaborative µElectronic Design Excellence Centre (CEDEC). Arjuna is also a Professional Engineer registered with The Society of Professional Engineers UK (A10503).

Selected Publications

Rasmi, A.[a] , Marzuki, A.[b] , Osman, M.N.[a] , Rahim, A.I.A.[a] , Yahya, M.R.[a] , Awang Mat, A.F.[a]
Development of 2.4 and 3.5 GHz 0.15mm GaAs PHEMT medium-power amplifier employing core-based design approach
(2010) *Microelectronics International*, 27 (1), pp. 25-32.

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Abstract
Purpose - The purpose of this paper is to discuss medium-power amplifier (MPA) design using parasitic-aware core-based approach. Design/methodology/ approach - This paper discusses a core-based design approach, which can also deliver multi-band radio frequency integrated circuit. Findings - A fabricated 3.5 GHz MPA achieved a P1dB of 16.81 dBm, power-added efficiency (PAE) of 16.74 percent and gain of 6.81 dB at the 10 dBm of input power under a low-power supply of 3 V. The maximum current, Imax is

80.7 mA and the power consumption of the device is 242.10mW. A fabricated 2.4 GHz MPA achieved a P1dB of 14.83 dBm, PAE of 11.73 percent and gain of 9.83 dB at the 5.0 dBm of input power under a low-power supply of 3.0 V. The maximum current, Imax is 84.4 mA and the power consumption for this device is 253.20mW. Originality/value - This paper shows the merits of the parasitic-aware design methods used in designing the core circuit.

Author Keywords
Amplifiers; Electronic engineering; Integrated circuits; Transistors

Document Type: Article
Source: Scopus

Rasmi, A.[a] , Marzuki, A.[b] , Abd Rahim, A.I.[a] , Razman Yahya, M.[a] , Fatah Awang Mat, A.[a]

A 3.5 GHz medium power amplifier using 0.15 µm GaAs PHEMT for WiMAX applications

(2009) *APMC 2009 - Asia Pacific Microwave Conference 2009*, art. no. 5385387, pp. 277-280.

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Abstract
This paper presents the design and measurement of a single-ended medium power amplifier (MPA) using 0.15 µm GaAs PHEMT technology for 802.16 WiMAX applications. At a supply voltage of 3.0V and 3.5 GHz operating frequency, a single-ended MPA achieves input return loss of 14.11 dB, output return loss of 12.38 dB, small-signal gain (S21) of 8.34 dB, P1dB of 16.81 dBm, power gain of 6.81 dB and the PAE of 16.74%. The die size of this amplifier is 1.2mm x 0.7mm. The maximum current, I_{max} is 80.70 mA and the power consumption of the device is 242.10 mW.

Author Keywords
3.5 GHz; GaAs PHEMT; Power amplifier; WiMAX applications

Document Type: Conference Paper
Source: Scopus

Maisurah M.H., S.[a] , Nizam O., M.[a] , Marzuki, A.[b] , Abdul Rahim, A.I.[a] , Razman Y., M.[a]
Characterization of on-wafer RF passive components for RFIC devices using three-steps de-embedding method
(2009) *Proceedings - MICC 2009: 2009 IEEE 9th Malaysia International Conference on Communications with a Special Workshop on Digital TV Contents*, art.
no. 5431531, pp. 362-366.

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Abstract
This paper demonstrates the process of characterizing on-wafer RF components for RFIC devices by using a three-steps de-embedding method. Three RF passive components are used for this purpose: spiral inductor, metalfinger capacitor and silicide-block N-poly resistor. The DUTs together with their calibration structure was fabricated in 0.13 µm CMOS technology. Comparisons between the simulated data, raw measured data and de-embedded data were made in order to see the accuracy of the de-embedding method. ©2009 IEEE.

Author Keywords
Calibration; Characterization; CMOS; De-embedding; RFIC

Document Type: Conference Paper
Source: Scopus

Farid, N.E.[a] , Marzuki, A.[b] , Rahim, A.I.A.[a]
A variable gain, 2.5 GHz CMOS low-noise amplifier for mobile wireless communications
(2009) *Proceedings - MICC 2009: 2009 IEEE 9th Malaysia International Conference on Communications with a Special Workshop on Digital TV Contents*, art.
no. 5431457, pp. 885-889.

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Abstract
A two-stage, variable-gain low-noise amplifier (LNA) which offers good matching and good noise performance is demonstrated. A prototype 2.5 GHz LNA is designed and

simulated using 0.13 um RF CMOS process technology. The simulated LNA has a maximum gain of 32.6 dB, input return loss of -44.9 dB, and output return loss of -5 dB. It has a noise figure of 1 dB and input P1dB of -33.9 dBm in high-gain mode, and noise figure of 2.6 dB and input P1dB of -14.6 dBm in lowgain (15.4 dB) mode. The complete device draws 20.3 mA of current from a 1.2 V supply for a total power consumption of 24.4 mW.

Author Keywords
Attenuator; CMOS; Input and output match; Low-noise amplifier; Noise figure; Receiver; Transceiver; Variable gain

Document Type: Conference Paper
Source: Scopus

Sanusi, R.[a] , Norhapizin, K.[a] , Rahim, S.A.E.Ab.[a] , Abdul Rahim, A.I.[a] , Marzuki, A.[b] , Yahya, M.R.[a]

Scalable MIM capacitor polynomial equation model development with application in the design of 2.4GHz PHEMT low noise amplifier

(2009) *APMC 2009 - Asia Pacific Microwave Conference 2009*, art. no. 5385221, pp. 2518-2521.

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Abstract
This paper presents the performance of scalable polynomial equation for very wide range of metal-insulator-metal (MIM) capacitor value which is obtained through curve fitting or optimization technique. It is used to describe the behavior of lumped element circuit model that has the same characteristic as the measurement data. The scalable polynomial equation is developed based on lumped element circuit model for frequency range of 0.8 GHz up to 18 GHz. Finally, 4 different scalable polynomial equations are derived, and applied in 2.4 GHz LNA circuit design for model verification.

Author Keywords
Equivalent circuit model; Gallium arsenide (GaAS); MIM capacitor; Model verification; Optimization; Polynomial equations; Scalable

Document Type: Conference Paper
Source: Scopus

Tang, S.C., Marzuki, A.
Design of Gilbert cell mixer in 0.18 µm CMOS technology and IF filter for FM receiver (2009) *SCOReD2009 - Proceedings of 2009 IEEE Student Conference on Research and Development*, art. no. 5443020, pp. 288-291.

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Abstract
This paper describes a doubly balanced Gilbert Cell mixer designed in CMOS technology. A 100 mV input signal was applied at both RF and LO port at different frequencies and their simulation curves were studied, the output voltage is approximately 300 mV. Gilbert cell mixer was designed till to the layout. For the IF filter, passive elements were studied. ©2009 IEEE.

Author Keywords
CMOS; Integrated circui; Mixer

Document Type: Conference Paper
Source: Scopus

Marzuki, A.[a] , Md. Shakaff, A.[b] , Sauli, Z.[c]
A 1.5 V, 0.85-13.35 GHZ MMIC low noise amplifier design using optimization technique (2009) *IETE Journal of Research*, 55 (6), pp. 309-314.

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Abstract
This paper describes how a broadband, 1.5 V, 0.85-13.35 GHz low noise amplifier in 0.15 µm 85 GHz PHEMT process is synthesized to simultaneously meet multiple design specifications such as bandwidth, noise figure, power gain and power consumption. Power-constrained synthesis technique is used to design the broadband amplifier. The simulated peak S21 is 19.8 dB, maximum noise Figure is 2.5 dB, 3-dB bandwidth is 12.5 GHz and power consumption is 73.5 mW. The calculated Figure of merit (FOM) is better than many reported broadband low noise amplifier (LNA).

Author Keywords
Broadband amplifier; Integrated circuit; Monolithic microwave integrated circuit; Optimization; Power-constrained; Pseudomorphic high electron mobility transistor

Document Type: Article
Source: Scopus

Neoh, S.C.[a] , Morad, N.[b] , Marzuki, A.[a] , Lim, C.P.[a] , Aziz, Z.A.[a]
A multi-resolution GA-PSO layered encoding cascade optimization model
(2009) *Studies in Computational Intelligence*, 248, pp. 121-140.

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Abstract
Many real-world problems involve optimization of multi-resolution parameters. In optimization problems, the higher the resolution, the larger the search space, and resolution affects the accuracy and performance of an optimization model. This article presents a genetic algorithm and particle swarm based cascade multi-resolution optimization model, and it is known as GA-PSO LECO. GA and PSO are combined in this research to integrate random as well as directional search to promote global exploration and local exploitation of solutions. The model is developed using the layered encoding representation structure, and is evaluated using two parameter optimization problems, i.e., the Tennessee Eastman chemical process optimization and the MMIC amplifier design interactive optimization.

Document Type: Article
Source: Scopus

Neoh, S.C.[a] , Marzuki, A.[a] , Morad, N.[b] , Lim, C.P.[a] , Aziz, Z.A.[a]
An interactive evolutionary algorithm for MMIC low noise amplifier design
(2009) *ICIC Express Letters*, 3 (1), pp. 15-19.

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Abstract
A layer-encoded interactive evolutionary algorithm (IEA) for optimization of design parameters of a monolithic microwave integrated circuit (MMIC) low noise amplifier is presented. The IEA comprises a combination of the genetic algorithm (GA) and the particle swarm optimization (PSO) technique. The layer-encoding structure allows human intervention in order to accelerate the process of evolution, whereas the GA and PSO technique are incorporated to enhance both global and local searches. With this combination of features, the proposed IEA has shown to be efficient in meeting all requirements and constraints of the MMIC. In addition, the IEA is able to optimize noise figure, current, and power gain of the MMIC amplifier design.

Author Keywords
Genetic algorithm; Interactive evolutionary algorithm; Layer encoding; MMIC design; Particle swarm optimization

Document Type: Article
Source: Scopus

Sanusi, R.[a] , Ismail, M.A.[a] , Norhapizin K.[a] , Rahim, A.I.A.[a] , Marzuki, A.[b] , Yahya, M.R.[a]
15 GHz SPDT switch design using 0.15 µm GaAs technology for microwave applications
(2008) *2008 International Conference on Electronic Design, ICED 2008*, art. no. 4786675, .

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Abstract
In this paper, very low loss and high isolation single pole double throw (SPDT) switch design for microwave applications using pseudomorphic high-electron mobility transistor (pHEMT) is presented. The MMIC switch design is developed using a commercially available 0.15 µm GaAs pHEMT technology. At the operating frequency of 15 GHz, the SPDT switch has 1.89 dB insertion loss and 26.66 dB of isolation. It also demonstrates 28.8 dBm of input P1dB gain compression point (P_{1db}) and 25.9 dBm of output P1dB. ©2008 IEEE.

Document Type: Conference Paper
Source: Scopus

Norhapizin, K.[a] , Ismail, M.A.[a] , Ahmad Ismat, A.R.[a] , Marzuki, A.[b] , Yahya, M.R.[a] , Mat, A.F.A.[a]

Parasitic effects of spiral inductors on the performance of GaAs-based MMIC low noise amplifier

(2008) *IEEE International Conference on Semiconductor Electronics, Proceedings, ICSE*, art. no. 4770293, pp. 134-137.

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Abstract
This paper is discusses about parasitic effect of spiral inductors on 5.8 GHz low noise amplifier (LNA) performances based on 0.5 µm GaAs pHEMT technology. Using S-parameter simulation, performance of the LNA between lump and distributed circuit are compared at 5.8 GHz. Electrical performance of the LNA performances by placing ideal components with non-ideal components shows that noise figure is increased by 2.31 dB, gain is decreased by 11.38 dB and input and output return loss is increased by 0.31 dB and 4.31 dB respectively. By using non-ideal components in the lump circuit analysis, it is shown that the spiral inductor has a noticeable impact on the LNA performance. The parasitic effects including self resonance on spiral inductors is discussed. This analysis is essential to ensure the simulation results yield realistic measured results for the fabricated LNA. Therefore the designer will have a good estimation on the performance of the LNA performance during the design stage prior to the testing stage. ©2008 IEEE.

Document Type: Conference Paper
Source: Scopus

Siti Maisurah, M.H.[a] , Marzuki, A.[b] , Mohd Azmi, I.[a] , Abdul Rahim, A.I.[a] , Mohamed Razman, Y.[a]

Design of 900MHz voltage-controlled oscillator using 0.18µm CMOS technology

(2008) *IEEE International Conference on Semiconductor Electronics, Proceedings, ICSE*, art. no. 4770364, pp. 462-465.

[a] TM Research and Development, TMR and D Innovation Centre, Lingkaran Teknokrat Timur, 63000 Cyberjaya, Selangor Darul Ehsan, Malaysia
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Abstract
This paper presents the design of a 900MHz LC oscillator implemented in 0.18µm RF

CMOS technology. Employing an on-chip PN varactor together with an on-chip spiral inductor, this Voltage-Controlled Oscillator (VCO) achieves a simulated phase noise of -100.9dBc/Hz at a 100kHz offset. The output frequency of the VCO can be tuned from 785MHz to 955.6MHz which correspond to 170.6MHz tuning range, obtained by only tuning the control voltage to the diode varactor pairs. The VCO consumes 6.5mW power from 1.6V DC supply voltage.

Document Type: Conference Paper
Source: Scopus

Marzuki, A.[a] , Shakaff, A.Y.M.[b] , Sauli, Z.[b]

Design of I/Q demodulator for W-CDMA

(2008) *IEEE International Conference on Semiconductor Electronics, Proceedings, ICSE*, art. no. 4770285, pp. 99-102.

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Abstract
The design of an InphaseQuadrature (I/Q) demodulator with low current consumption is described. The I/Q demodulator was designed for Wideband code division multiple access (W-CDMA) communication system. SiGe 0.35µm BiCMOS technology with f_T =45GHz, f_{max} =60GHz and Noise Figure = 0.8dB at 2GHz was used for the design. A top-down and bottom-up approach was used in designing the I/Q demodulator. CMOS devices were primarily used in the biasing circuits for power consumption reduction while SiGe Bipolar devices were used in signal path circuits. The design contained 2 mixers, a local oscillator (LO) divider, negative resistance circuit, buffer amplifiers and bias/control circuits. The I/Q demodulator circuits were then layout and had gone through the postlayout simulation to check performance with the parasitic elements which were introduced from the layout. A design prototype was measured and was found to be agreed with the simulation results. The prototype worked in the region of 190 MHz input frequency and 0 - 35MHz output frequency. The prototype had also met the specifications for the WCDMA hand phone receiver. It achieves EVM of 2.9 %. It is also achieved gain ripple of 0.12 dB, gain mismatch of 0.1 dB and phase mismatch of 1.25°. Finally, the design which is consisted of mixers, frequency dividers, VCO buffer amplifiers and bias/control circuits consumes 4 mA with 3 V power supply. ©2008 IEEE.

Author Keywords
Demodulator; Integrated circuit; W-CDMA

Document Type: Conference Paper
Source: Scopus

Marzuki, A.[a] , Khor, T.T.[a] , Sauli, Z.[b] , Shakaff, A.Y.M.[b]

Ultra-wideband variable signal generator using series shunt switch

(2008) *IEEE Region 10 Annual International Conference, Proceedings/TENCON*, art. no. 4766418, .

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Abstract
Ultra-Wideband (UWB) technologies are at the forefront of wireless communications, offering the possibility to provide extremely high data rate wireless solutions. This paper works on the UWB variable signal generator that is capable of fast switching between different center frequencies. The target switching time is 4ns and the three center frequencies at the lower band are selected, which are 3.35GHz, 3.85GHz and 4.35GHz. The structure of our variable signal generator is based on the topology of active oscillators. By using a switching network, the different frequencies from different local oscillators are switched within 4ns. In this project, a basic NMOS switch is studied and the weaknesses are justified. A new topology of NMOS switch based on series-shunt configuration is proposed so that it is able to pass the signal from oscillators to output without transition spike. Three oscillators operating at targeted center frequencies are designed based on crosscoupled LC topology. The problems and issues after the integration of switches and oscillators are identified and solved. A modified switch is developed specially for solving the loading effect design issue. By optimizing the transistor size for switch and other design parameters in oscillator, it is possible to generate the signal at desired frequency and amplitude without transition noise. The performance of our variable signal generator is estimated through simulation with a target technology of Silterra 0.18 μm CMOS at a supply voltage of 1.8 V. The simulation results indicate that our variable signal generator is able to produce a signal with three center frequencies, i.e. 3.35GHz, 3.85GHz and 4.35GHz at 400mV peak-to-peak swing within every 4ns.

Author Keywords
NMOS switch; Oscillator; UWB

Document Type: Conference Paper
Source: Scopus

Sanusi, R.[a] , Ismail, M.A.[a] , Norhapizin, K.[a] , Abdul Rahim, A.I.[a] , Marzuki, A.[b] , Yahya, M.R.[a]

30 GHz SPDT switch design using 0.15 µm GaAs technology for microwave applications

(2008) *IEEE International Conference on Semiconductor Electronics, Proceedings, ICSE*, art. no. 4770292, pp. 130-133.

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Abstract
In this paper, very low loss and high isolation single pole double throw (SPDT) switch design for millimeter wave applications using pseudomorphic high-electron mobility transistor (pHEMT) is presented. The MMIC switch design is developed using a commercial 0.15 µm GaAs pHEMT technology. At the operating frequency of 30 GHz, the SPDT switch has 1.948 dB insertion loss and 24.526 dB of isolation. It also demonstrates 26.85 dBm of input P1dB gain compression point (P_{ldB}) and 23.28 dBm of output P1dB. ©2008 IEEE.

Document Type: Conference Paper
Source: Scopus

Rasmi, A.[a] , Marzuki, A.[b] , Ismail, M.A.[a] , Abdul Rahim, A.I.[a] , Yahya, M.R.[a] , Awang Mat, A.F.[a]

0.5 µm gaAs PHEMT medium power amplifier design using simple RC feedback amplifier for wireless LAN applications

(2008) *Proceedings of 2008 Asia Pacific Microwave Conference, APMC 2008*, art. no. 4958373, .

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Document Type: Conference Paper
Source: Scopus

Rasmi, A.[a] , Marzuki, A.[b] , Ismail, M.A.[a] , Rahim, A.I.A.[a] , Yahya, M.R.[a] , Mat, A.F.A.[a]

Design of 2-stage medium power amplifier using 0.5 µm GaAs PHEMT for wireless LAN

applications
(2008) *IEEE Region 10 Annual International Conference, Proceedings/TENCON*, art. no. 4766538, .

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Abstract
This paper presents the design and fabrication of two-stage medium power amplifier (MPA) using 0.5 µm GaAs PHEMT technology for the wireless LAN applications. The die size of this amplifier is only 1.7mm x 0.85mm. At a supply voltage of 5.0Vand 5.8 GHz operating frequency, a 2-stage MPA achieves a linear gain (S21) of 16.39 dB, P1dB of 20.18dBm, power gain of 15.15 dB and the PAE of 25.29%.

Author Keywords
2-stage MPA; 5.8 GHz; GaAs PHEMT; Wireless LAN applications

Document Type: Conference Paper
Source: Scopus

Neoh, S.C., Marzuki, A., Morad, N., Lim, C.P., Aziz, Z.A.
An interactive genetic algorithm approach to MMIC low noise amplifier design using a layered encoding structure
(2008) *2008 IEEE Congress on Evolutionary Computation, CEC 2008*, art. no. 4631001, pp. 1571-1575. Cited 1 time.

Abstract
In this paper, an interactive genetic algorithm (IGA) approach is developed to optimize design variables for a monolithic microwave integrated circuit (MMIC) low noise amplifier. A layered encoding structure is employed to the problem representation in genetic algorithm to allow human intervention in the circuit design variable tuning process. The MMIC amplifier design is synthesized using the Agilent Advance Design System (ADS), and the IGA is proposed to tune the design variables in order to meet multiple constraints and objectives such as noise figure, current and simulated power gain. The developed IGA is compared with other optimization techniques from ADS. The results showed that the IGA performs better in achieving most of the involved objectives. © 2008 IEEE.

Document Type: Conference Paper
Source: Scopus

Marzuki, A.[a] , Sauli, Z.[b] , Shakaff, A.Y.M.[c]
A voltage reference circuit for current source of RFIC blocks
(2008) *Microelectronics International*, 25 (3), pp. 26-32. Cited 1 time.

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Abstract
Purpose - The purpose of this paper is to design a voltage reference circuit for current source of radio frequency integrated circuit blocks. The voltage reference circuit is called voltage for current source (VCS). Design/methodology/approach - The circuit concept is discussed. A voltage-controlled oscillator (VCO) and buffer circuit together with VCS circuit are built to prove the concept. Though the VCS circuit employs no array of diode like standard bandgap circuit, it still employs the concept of proportional to absolute temperature (PTAT) and a complement to absolute temperature (CTAT) elements. The integrated VCO, together with VCO core and VCO buffer circuits, are designed for W-CDMA application particularly for the demodulator section. All circuits are built in f_T=45 GHz SiGe BiCMOS process. Findings - At 760 MHz the power consumption for core circuit is 0.6 and 3.3 mA for VCO buffer amplifier. The fabricated VCO circuit together with VCO buffer was tested and measured with VCO output of -6 dBm at 760 MHz with variation of 0.1 dBm across -40°C to 85°C. Originality/value - A voltage reference circuit which is derived from PTAT and CTAT current generators is presented. The circuit is capable of providing a constant current across absolute temperature or a current PTAT. © Emerald Group Publishing Limited.

Author Keywords
Electric current; Oscillators; Radio frequencies; Semiconductor devices; Temperature; Voltage

Document Type: Article
Source: Scopus

Marzuki, A.[a d] , Rasmi, A.[b] , Sauli, Z.[c] , Shakaff, A.Y.M.[c]
Core-based design with parasitic-aware approach for medium power amplifier at 900 MHz, 2.4 GHz, 3.5 GHz and 5.85 GHz
(2008) *Informacije MIDEM*, 38 (2), pp. 131-139. Cited 1 time.

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Abstract
Practical core-based design suitable for medium power amplifier (MPA) is presented. The core circuit is developed and applied at 0.9 GHz, 2.4 GHz, 3.5 GHz and 5.85 GHz. Parasitic-aware design flow is introduced in the whole approach. 5.85 GHz MPA achieves a P1 dB of 16.5 dBm, PAE of 15.8% and gain of 4.5 dB at the 12 dBm power input under a low power supply of 2.5V. The maximum current, Im8x is 77 mA and the power consumption of the device is 192.50 mW. 3.5 GHz MPA achieves a P1 dB of 18.2 dBm, PAE of 26.5% and gain of 7.98 dB at the 10.2 dBm power input under a low power supply of 3.0V. The maximum current, I_{max} is 79 mA and the power consumption of the device is 237 mW. 2.4 GHz MPA achieves a P1 dB of 17 dBm, PAE of 20.1 % and gain of 7.0 dB at the 10 dBm power input under a low power supply of 3.0V. The maximum current, Imax is 79 mA and the power consumption of the device is 237 mW. 0.9 GHz MPA achieves a P1 dB of 14.2 dBm, PAE of 11 % and gain of 4.2 dB at the 10 dBm power input under a low power supply of 3.0 V. The maximum current, I_{max} is 79 mA and the power consumption of the device is 237 mW. Lastly, simulated results almost match the measurement results shows the advantages of applying parasitic information to the core circuit for MPA designs and the effectiveness of core-based design approach in Radio Frequency Integrated Circuit (RFIC) and Monolithic Microwave Integrated Circuit (MMIC).

Author Keywords
Medium power amplifier; MMIC; Parasitic aware approach; RFIC

Document Type: Article
Source: Scopus

Marzuki, A.[a] , David, S.[b]
Design of 920 MHz, 0.8 µm CMOS low noise amplifier for UHF RFID reader
(2006) *2006 International RF and Microwave Conference, (RFM) Proceedings*, art. no. 4133572, pp. 149-151.

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Abstract
A 920 MHz low noise amplifier (LNA) design for UHF RFID reader application, requiring one external inductor and matched to 50 Ω at the output, has been implemented in a standard analog 0.8-µm CMOS technology. Cascode topology is used in the design provide good gain and moderate noise figure. High frequency inductor model is also presented. Simulated noise figures for the LNA are 2.02 dB at 197 mW, and 2.81 dB at 28.2 mW. The LNA has a power gain of 15.7 dB, and an IIP3 of 3 dBm at 197 mW. The LNA has a power gain of 12.46 dB, and an IIP3 of 2.61 dBm at 28.2 mW. © 2006 IEEE.

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Marzuki, A., Zulkifli, T.Z.A., Noh, N.M., Aziz, Z.A.A.
A broadband RF feedback amplifier design with simple feedback network
(2004) *2004 RF and Microwave Conference, RFM 2004 - Proceedings*, pp. 1-4. Cited 7 times.

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Abstract
This paper presents a simple and fast design technique of a RF feedback amplifier. The amplifier uses a series of resistor and capacitor as the feedback element. An overview of the amplifier impedance analysis and noise theory of the amplifier will be presented. High frequency model of passive component will also be presented. With a current consumption of 6mA the simulated amplifier features a noise figure of 2.4dB and a S₂₁ of 14.7dB at 2GHz. It achieves considerably flat S₂₁ across 50MHz to 2.5GHz. © 2004 IEEE.

Document Type: Conference Paper
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