Layout and Memory

Stick DiagramType of memory



IC Layout

- The physical (mask layout) design of CMOS logic gates is an iterative process.
- If the logic gate contains more than 4-6 transistors, the topological graph representation and the Euler-path method allow the designer to determine the optimum ordering of the transistors.
- A simple stick diagram layout can now be drawn, showing the locations of the transistors, the local interconnections between the transistors and the locations of the contacts.



Pull-up Graph





CMOS Logic





CMOS Loaic



pMOS network graph



nMOS network







nMOS network

pMOS network

The Euler path is defined as an uninterrupted path that traverses each edge (branch) of the graph exactly once















- Static RAM is faster and holds data as long as power supply is attached.
- Dynamic RAM provides a higher integration level.



• Static RAM (SRAM);

- fast;
- low capacity;
- simple interface (no additional circuits supporting prolonged holding of data).
- Dynamic RAM (DRAM) detailed description follows;
 - very high capacity;
 - needs constant refreshing of data (each 10-20ms);
 - complicated interface;
 - row and column address select signals; once a row is selected, it gets "refreshed".



• Nonvolatile RAM (NVRAM);

- battery-backed;
- very fast (as SRAM);
- no limit on the number of cell rewritings;
- no special programming needed;







ROMs







ROMs



- Mask programmable ROM
 - Pre-programmed at fabrication
- One-time programmable ROM
 - Fuses blown during programming
- Erasable programmable ROM (EPROM)
 - use MOS transistors with isoating gate.
 - Programming ~ electrons are injected into the foating gate; this keeps the transistor constantly open.
 - Erasing ~ electrons escape the gate when the potential barrier is lowered by means of UV radiation; this forces the transistor to stay closed.