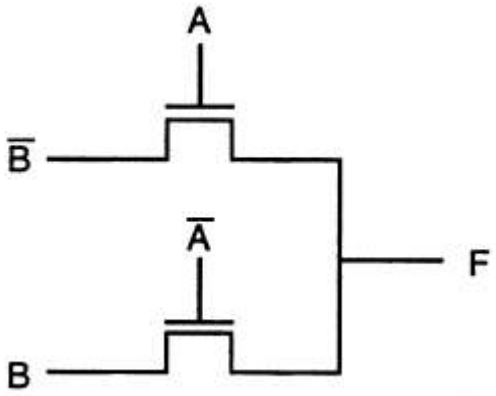
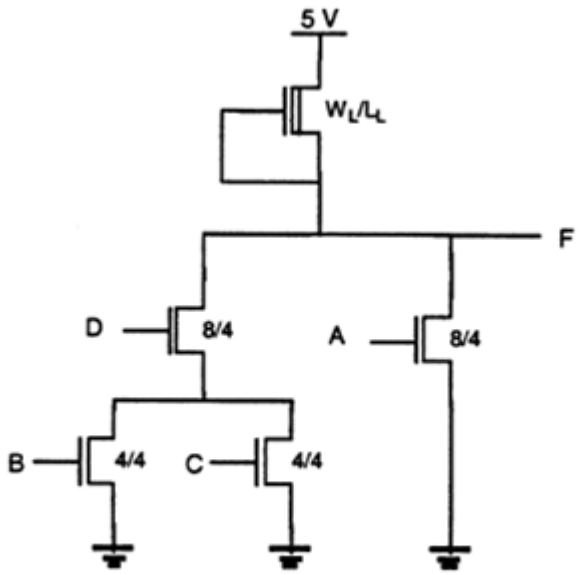


4. (a). Determine Logic Function F.
Tentukan rangkap logic F. (4 pts)

(b). Design a circuit to implement the same logic function, but using NOR gates. Draw a transistor-level schematic and use NMOS Enhancement-Depletion technology.
Dengan menggunakan get TAK ATAU, reka litar yang mempunyai rangkap logic yang sama. Lukis skema aras transistor dan guna teknologi peningkatan-kesusutan NMOS. (8 pts)

(c). Design a circuit to implement the same logic function, but using AND-OR-INVERT gate. Draw a transistor level schematic and use CMOS technology.
Dengan menggunakan get DAN-ATAU-SONSANG, reka litar yang mempunyai rangkap logic yang sama. Lukis skema aras transistor dan guna teknologi CMOS. (8 pts)

5.(a). Calculate W_L/L_L such that V_{OL} does not exceed 0.3 V.
$V_{T,load} = -3V$, $V_{T,driver} = 1$ V
Kira W_L/L_L bagi V_{OL} tidak lebih daripada 0.3 V. (7 pts)
$V_{T,load} = -3V$, $V_{T,driver} = 1$ V



(b). Draw stick diagram for the above circuit.
Lukis gambarajah lidi untuk litar di atas. (6 pts)

(c). Design and draw an 8-bit serial to parallel converter using flip-flop.
Reka dan lukis penukar siri kepada selari 8-bit menggunakan flip-flop. (7pts).

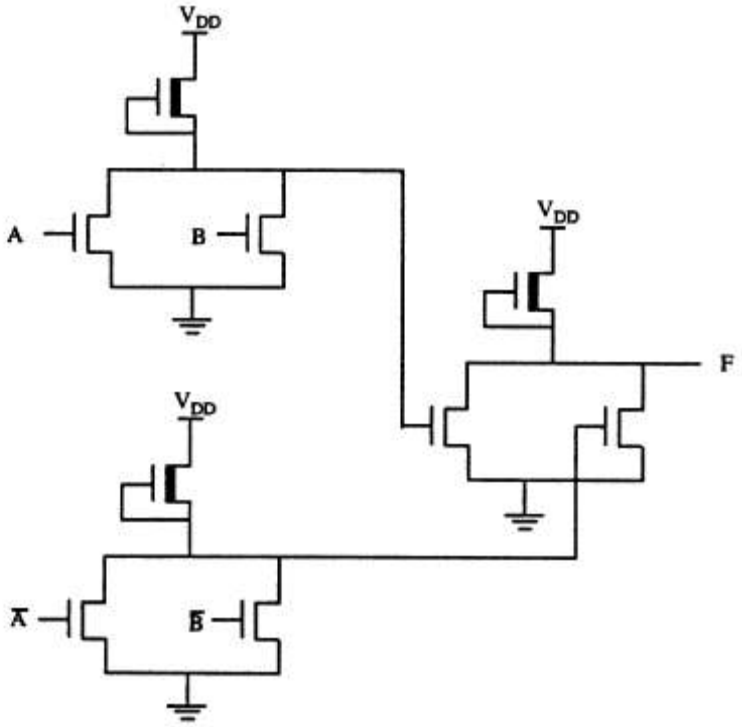
Solutions.

4. (a).

$$F = A\overline{B} + \overline{A}B = A \oplus B$$

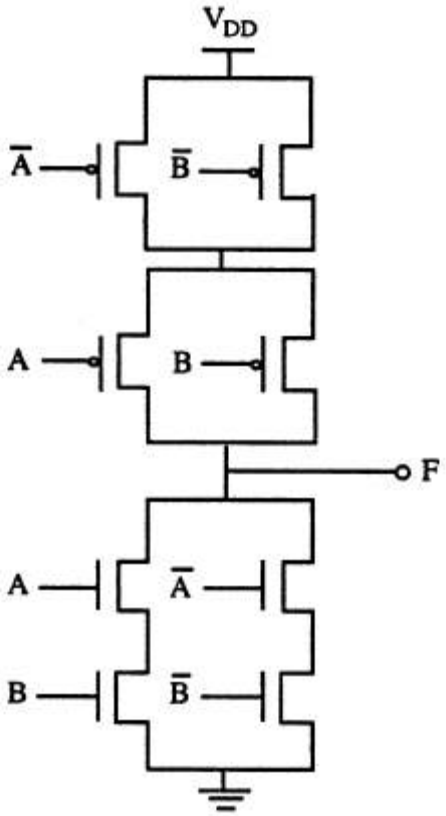
(b).

$$F = A\overline{B} + \overline{A}B = (A+B)\left(\overline{A}+\overline{B}\right) = \overline{\overline{(A+B)} + \overline{(\overline{A}+\overline{B})}}$$



(c).

$$\overline{F} = AB + \overline{A}\,\overline{B}$$
$$F = \overline{\overline{F}} = \overline{AB + \overline{A}\,\overline{B}}$$



5 (a).

(b) V_{OL} maximum occurs when A=1, D=0 and either (but not both) B=1 or C=1. Under these conditions, the circuit may be simplified as a depletion load inverter with the equivalent driver W/L given below.

$$\left.\frac{L}{W}\right|_{equiv} = \frac{4}{8} + \frac{4}{4} = \frac{3}{2}$$

$$\therefore \left.\frac{W}{L}\right|_{equiv} = \frac{2}{3}$$

When V_{OL} = 0.3 V, V_{IN} = 5V, the load in saturated and driver in linear region.

$$\frac{k'}{2}\left(\frac{W}{L}\right)_{load}\left(V_{GS,load}-V_{T,load}\right)^2 = k'\frac{2}{3}\left[(V_{IN}-V_{T,driver})V_{out}-\frac{1}{2}{V_{out}}^2\right]$$

$$\frac{k'}{2}\left(\frac{W}{L}\right)_{load}(0+3)^2 = k'\frac{2}{3}\left[(5-1)\times 0.3-\frac{1}{2}\times 0.3^2\right]$$

$(W/L)_{load}$ = 0.171

Therefore $(W/L)_{load} \le 0.171$ for $V_{OL} \le$ 0.3 V.

(b) poly A,B,C and D must vertically drawn. Each source/drain must be pointed clearly.
(c) Drawing should include at least 8 flip-flops. Triggering method and clocking method.