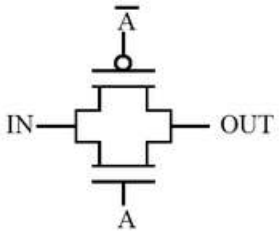


4. (a). Explain at least two applications of CMOS transmission gate.
Terangkan sekurang-kurangya dua kegunaan get hantaran CMOS. (4 pts)

(b). IF V_{IN} and V_A is V_{DD} explain the state of operation for NMOS and PMOS when $|V_{TP}|<V_{OUT}<|V_{DD}-V_{TN}|$
Sekiranya V_{IN} dan V_A adalah V_{DD}, terangkan operasi NMOS dan PMOS apabila $|V_{TP}|<V_{OUT}<|V_{DD}-V_{TN}|$
(8 pts)

(c). Draw the layout of the CMOS transmission gate efficiently.
Lukis bentangan bagi get hantaran CMOS yang efektif . (8 pts)

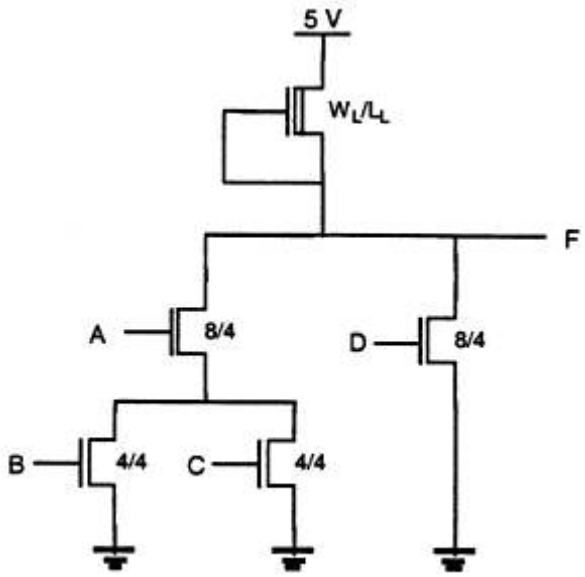
5

a). Determine logic function F. Tentukan logic F.

Kirakan W_L/L_L sekiranya V_{OL} tidak melebihi 0.3 V.

Calculate W_L/L_L such that V_{OL} does not exceed 0.3 V.

$V_{T,load} = -3V$, $V_{T,driver} = 1$ V (7pts).



(b). Draw stick diagram for the above circuit.
Lukis gambarajah lidi untuk litar di atas. (6 pts)

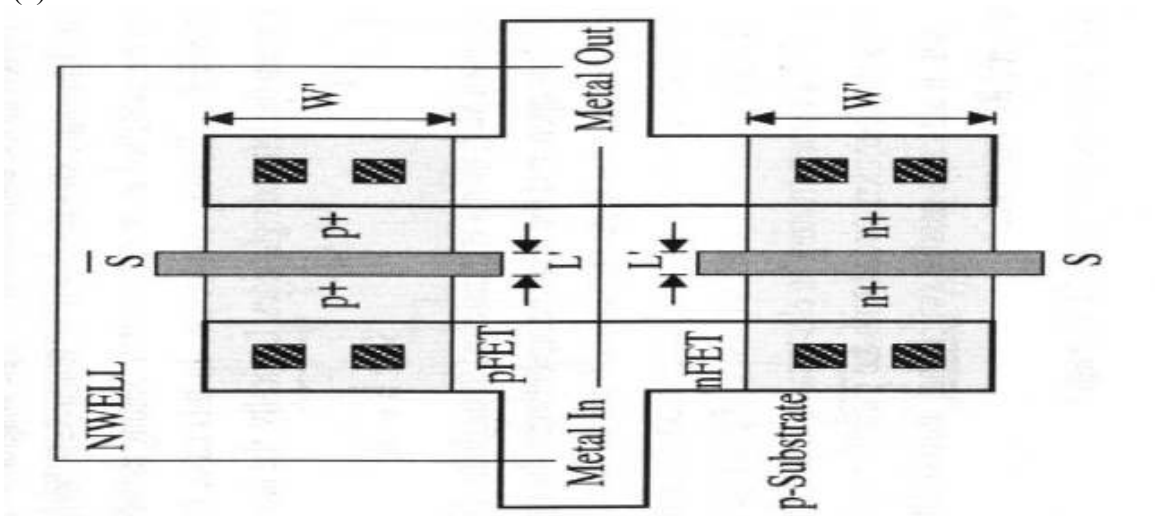
(c). Design and draw an 8-bit parallel to serial converter using flip-flop.
Reka dan lukis penukar selari kepada siri 8-bit menggunakan flip-flop. (7pts).

Solutions.

4(a). Combinational Logic gate and Switch.

(b). PMOS in linear region. NMOS in saturation region. Answer must be coupled with explanation using at least drain current equation.

(c).



5 (a).

(a) $F = \overline{A(B+C)+D}$

(b) V_{OL} maximum occurs when A=1, D=0 and either (but not both) B=1 or C=1. Under these conditions, the circuit may be simplified as a depletion load inverter with the equivalent driver W/L given below.

$$\left.\frac{L}{W}\right|_{equiv} = \frac{4}{8} + \frac{4}{4} = \frac{3}{2}$$

$$\therefore \left.\frac{W}{L}\right|_{equiv} = \frac{2}{3}$$

When $V_{OL} = 0.3$ V, $V_{IN} = 5$V, the load in saturated and driver in linear region.

$$\frac{k'}{2}\left(\frac{W}{L}\right)_{load}\left(V_{GS,load} - V_{T,load}\right)^2 = k'\frac{2}{3}\left[(V_{IN} - V_{T,driver})V_{out} - \frac{1}{2}V_{out}{}^2\right]$$

$$\frac{k'}{2}\left(\frac{W}{L}\right)_{load}(0+3)^2 = k'\frac{2}{3}\left[(5-1)\times 0.3 - \frac{1}{2}\times 0.3^2\right]$$

$(W/L)_{load} = 0.171$

Therefore $(W/L)_{load} \le 0.171$ for $V_{OL} \le 0.3$ V.

(b) poly A,B,C and D must vertically drawn. Each source/drain must be pointed clearly.
(c) Drawing should include at least 8 flip-flops. Triggering method and clocking method.