Feedback is a wonderful thing. We take the inverted output signal, subtract the input signal from it and the amplifier will automatically correct and difference between them. If we only feed back a fraction of the output signal, the amplifier will automatically adjust its gain to one over that fraction.

Using a single frequency (any frequency), inverting a signal (negative feedback) is the same as a 180 degree phase-shift. And here comes the problem: Each device in the amplifier has a little bit of delay. At low frequency this has little effect, but as we go higher and higher in frequency the delay becomes more and more noticeable. At some high frequency the delay amounts to half a period of the signal and thus causes a phase-shift of 180 degrees. What started out as negative feedback now becomes positive feedback and the whole thing oscillates.

Frequency compensation is a design method which avoids this. The principle is very simple: deliberately slow down one device so that it is much slower than all others, i.e. it dominates the frequency response so that the delay in all other devices is no longer important.

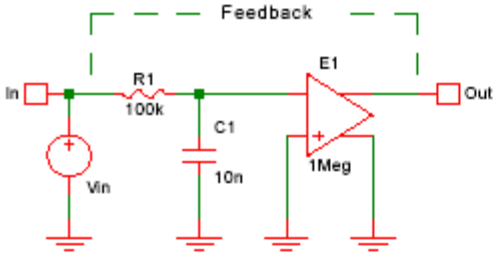

Fig. 6-8: Abstract circuit to illustrate phase-shift in a feedback amplifier.

This is illustrated with a very simple simulation. E1 is a "voltage-controlled voltage source" and acts like an ideal op-amp with a gain of 1 million (120dB), has no delay and the input and output terminals are free-floating (but are referenced here to ground). R1 and C1 cause the single delay (i.e. phase-shift).

Due to the RC network the amplitude at the output starts decreasing at about 100Hz. At this point the phase of the signal at the output is considerably less than 180 degrees, but as we go higher in frequency the phase never goes below 90 degrees. Thus the signal being fed back to the input cannot reach a phase-shift of zero degrees, the condition for

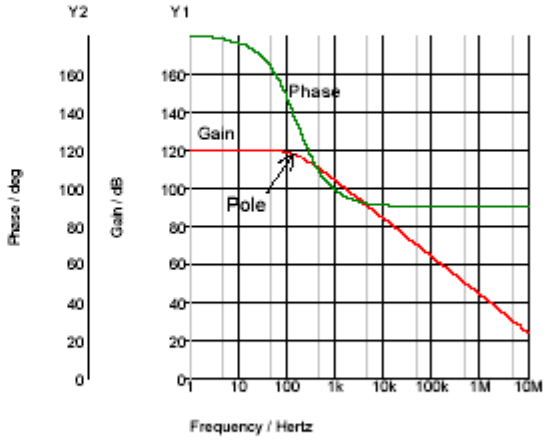

Fig. 6-9: Single-pole response. The phase never goes below 90 degrees.

oscillation.

The point at which the phase has turned by 45 degrees is called a pole. At frequencies somewhat higher than the pole the amplitude drops by 6dB per octave (doubling of frequency) or 20dB per decade.

Now let's look at the same simulation with another RC network added at the output, with a pole at a much higher frequency (C = 100pF). We now have two poles; you can just barely see the second pole (at about 10kHz) by the change in the steepness of the gain curve. The maximum phase-shift now is 180 degrees. The point of interest is the frequency at which the gain moves through zero dB (i.e. a gain of 1). If the gain is less than 1 an oscillation cannot sustain itself. While the phase at this point only approaches zero degrees, the margin is far too close for comfort.

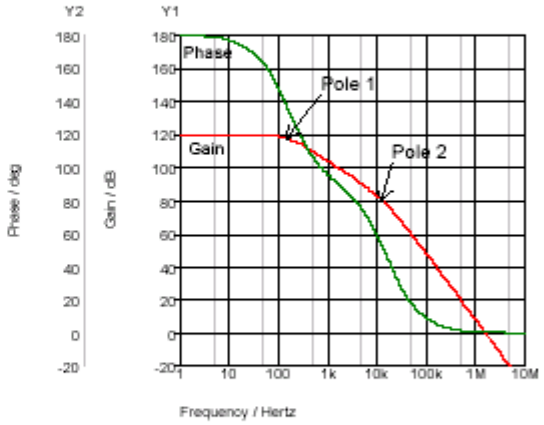

Fig. 6-10: Two poles in a feedback path approach zero degrees phase-shift.

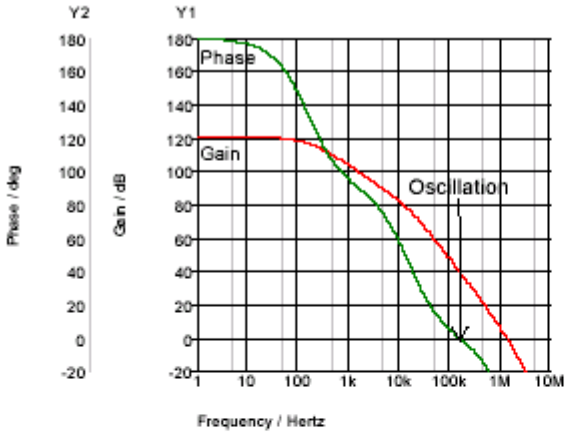

Fig. 6-11: Three poles in a feedback path. Phase-shift goes through zero degrees and oscillation takes place.

With three poles we are clearly out of luck. The phase now reaches zero degrees a decade before the gain drops below 0 dB. An amplifier which has these three poles will oscillate, in fact we can tell with certainty that it will oscillate at 200kHz.

There are now three remedies: 1. we can lower the gain until it drops below 0dB before the phase reaches zero degrees; 2. we can insert a new pole at a frequency so low that it dominates the others and 3. you can introduce a zero.

To illustrate the effect of a zero, we use another artificial circuit. R1/C1, R2/C2 and R3/C3 provide the three poles, delaying the phase of the signal, each by the same amount as in figure 6-11. R4, together with C2 provides the zero, it advances the phase rather than retarding it. The

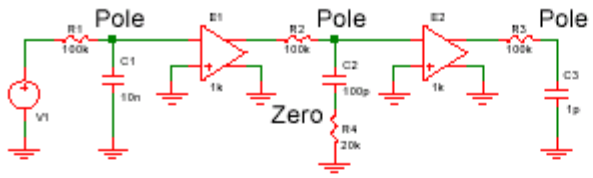

Fig. 6-12: Three poles and a zero.

(5MHz) the gain drops below 0dB but the phase is still positive, about 15 degrees, called the **phase margin**. Theoretically a feedback circuit with this behavior will not oscillate, though the phase margin is rather low. Since gain and time constants are subject to variation in an IC, it should be at least 60 degrees.

Now let's look at a real design, a simple, bipolar op-amp; this rather outdated

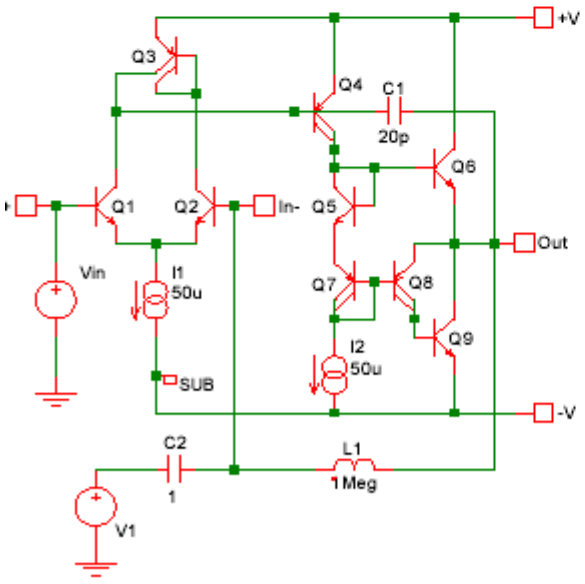

Fig. 6-14: Measuring gain and phase in a feedback loop.

frequency (i.e. the value of R4) is selected to result in a frequency where it is most effective.

At about 30kHz R4/C2 start turning back the phase, so that at the critical frequency

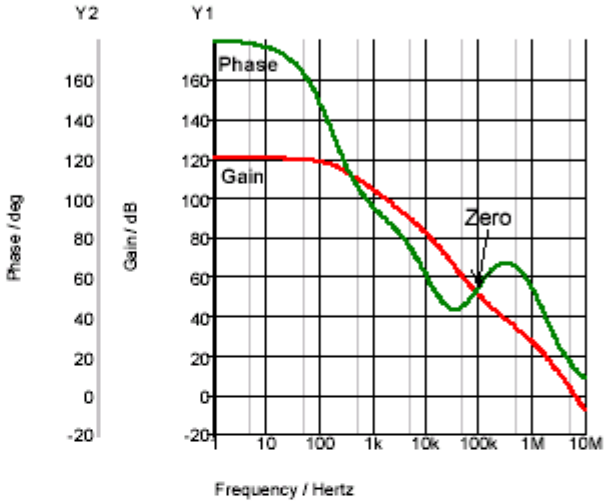

Fig. 6-13: A zero retards the phase-shift.

circuit was chosen because it uses the slow lateral PNP transistors, which aggravate the phase-shift problem beautifully.

The circuit uses the classical 3-stage design for op-amps (more of this in chapter 8): an input stage which converts the differential input signal to a single-ended one and has gain, a second stage (Q4) which provides more gain, and an output stage which has no (voltage) gain but provides a reasonably high output current. Since high-current PNP transistors are often not available in an IC, the lower portion of the output stage uses a compound transistor;

from the second stage it looks like a PNP transistor, from the output like an NPN one (but the combined device is achingly slow).

Q5 and Q7 are diode-connected transistors to bias Q6 and Q8.

The amplifier is investigated as a buffer, i.e. with a gain of one, produced by connecting the output directly to the inverting input. Here, though, there is an inductor in the path, which blocks AC but lets DC through so that the circuit is properly biased. C2, a very large capacitor, couples an AC signal to the negative input. In this way the feedback loop is opened up and we can measure loop gain and phase. This can be done at any convenient point in the loop, but the output to input connection is clearly the most convenient. Note that L1 and C2 have impractically large values. This is of no great consequence since these components are not going to be part on the design; we want to make sure they don't influence the AC behavior of the circuit.

We feed the AC signal into the loop after the inductor and then measure the loop response before the inductor (at "Out").

First let's look at the loop without C1. The loop gain is about 92dB and the phase drops rather sharply, reaching zero degrees long before the gain reaches 0dB. (Gain and phase have identical scales for easier reading). In fact, when the phase reaches zero degrees, the gain is still about 42dB. Therefore this circuit is unstable, it will oscillate.

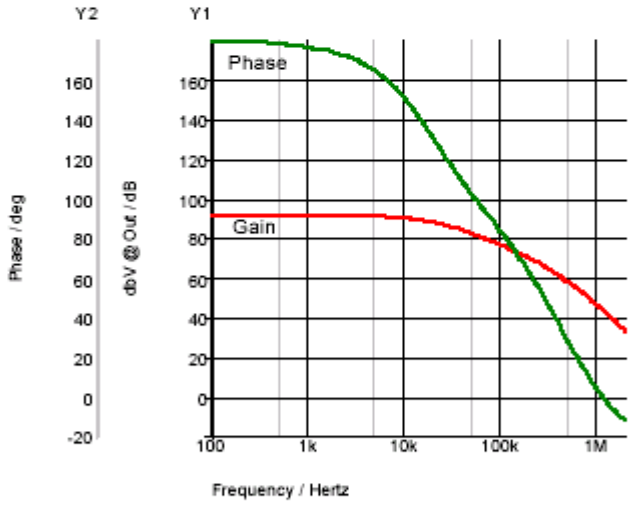

Fig. 6-15: Loop gain and phase of figure 6-14 without C1. The circuit would undoubtedly oscillate, the phase reaches zero degrees while there is still gain.

C1, the compensation capacitor, has been placed at the most strategic point in the circuit. There is considerable voltage gain between the base of Q4 and the output, which multiplies its apparent value (the Miller effect). Without this multiplication we would need a capacitor of about 2000pF, too large for an IC. It is also important that the capacitor feed back the AC signal from a reasonably low impedance (here the output) to a very high one (the current mirror and the base of Q4) so that we get nearly the full AC voltage swing at this point.

The result is self-evident. A new pole is created, about 100 times lower in frequency than the next higher one. This pole now dominates up to at least 10MHz and the phase is still 65 degrees away from zero when the gain drops below one. A stable circuit with an adequate safety margin.

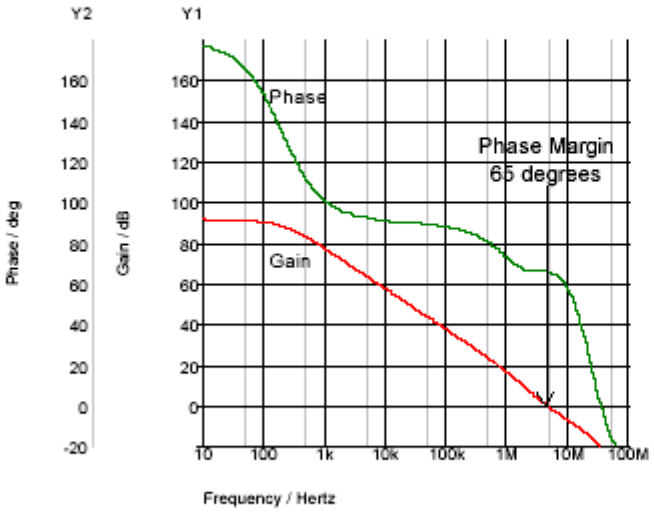

Fig. 6-16: With C1 the circuit of figure 6-14 has a phase margin of 65 degrees, i.e. the gain drops through 0dB safely before the phase reaches 0.

Of course there is a price to be paid for this stability: the gain of the op-amp may be more than 90dB at 10Hz, but it drops steadily as the operating frequency is increased. If we use this op-amp at 10kHz, we only have about 58dB of gain.

This analysis has assumed that the op-amp is going to be used with a gain of one. But if you are creating a design with a fixed gain, say 40dB, there is no reason why it should have to be stable at a gain of one. Which makes frequency compensation much less demanding. Just look at figure 6-15. Subtract 40dB from the gain curve (only the *excess* gain counts) and the amplifier is almost stable, i.e. a much smaller compensation capacitor is required.

The gain/phase analysis, as elegant and informative as it is, has a serious flaw: it shows performance only at one particular operating point (it is, after all, an AC analysis which does not disturb DC operating voltage and currents). A real-life signal will change the DC operating point and the loop gain and phase can change substantially.

Some simulators let you perform this AC analysis at different DC operating points, but there is an easier way , one that is a surefire test for stability. Get rid of the inductor and C2, close the feedback loop as intended in the application and apply a square-wave at the input. The square-wave should have fast edges (the default values in the simulator are adequate).

Then observe the output and watch for overshoot. For this circuit, with C1 at 20pF, there is a slight overshoot, one peak only. This circuit is very stable. (You can also see that the large compensation capacitor affects the slew-rate rather badly).

With the compensation capacitor reduced to 5pF there are three to four peaks, a damped oscillation. Up to four peaks are acceptable. If there are more, you are asking for trouble.

To make absolutely sure, do this with a brief (10 run) Monte Carlo Analysis at the temperature extremes and also for a rapidly varying load and supply voltage (less likely to cause instability, but it doesn't take much time to check). If there are never more than four peaks, you are safe.

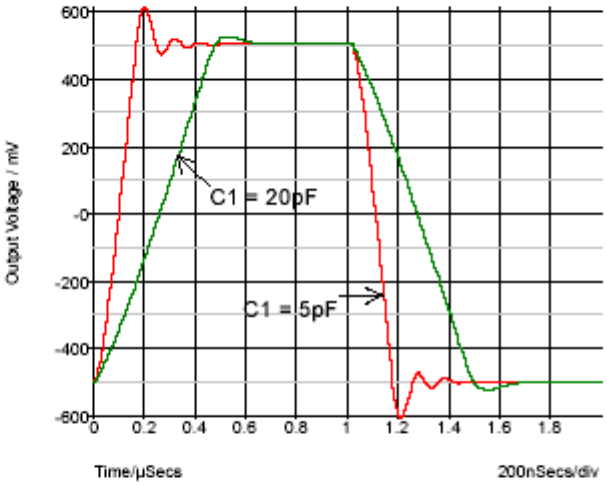

Fig. 6-17: To make sure a feedback circuit does not oscillate observe the pulse response. If there is ringing with fewer than 4 peaks, the circuit is stable.

A final small hint: in a gain/phase analysis simulators often get confused about the phase. You will see a plot which starts not at 180 degrees, but at -180. The two are in fact the same.