Lab 2-EEE 445

General Comments

Don't panic when you see the circuit. It looks overwhelming at first but it is made up of simple building-block pieces and it is understandable. In addition, you will be given help along the way, first by this write-up, and later in recitations, lectures, and additional handouts. At the same time, the design process you need to go through is a complex one and not one you will successfully negotiate in one sitting. Thus it is important that you get started, first developing an understanding of the circuit and the nature of the design challenge, and then at doing your design. You can do it, but not in one night.

Design Objective

Your design objective is to specify component values for the integrated linear amplifier shown in Figure 1 so that it meets or, hopefully, exceeds the performance objectives itemized below.

The circuit is a BiCMOS differential amplifier designed to have a large output voltage swing, large common-mode rejection ratio, and large common-mode input voltage range. It relies heavily on n-channel MOSFETs in the critical gain stages to maximize its bandwidth.

You are to specify the resistor values and certain device dimensions in the circuit in Figure 1, and to calculate the corresponding bias levels and performance characteristics.

REMEMBER: Please change Bipolar devices to CMOS devices!!!!

Performance Objectives:

1) Small-signal gains defined by writing $v_{out} = A_{vc}(v_{in1}+v_{in2})/2 + A_{vd}(v_{in1} - v_{in2})$:

i) Small-signal difference-mode voltage gain, $|A_{vd}|$: 5×10^{3}

ii) Small-signal common-mode voltage gain, $|A_{vc}|$: 5×10^{-4}

2) Common-mode rejection ratio, A_{vd}/A_{vc}: 10^{7}

3) Small-signal output resistance, r_{out}: 75 W.

4) Maximum output voltage swing into a 100 W load, $|v_{OUT}|_{max}$: 0.65 V.

5) Minimum common-mode input voltage range, $|v_{IC}|_{min}$: 0.5 V.

6) Total quiescent power dissipation not to exceed 5 mW.

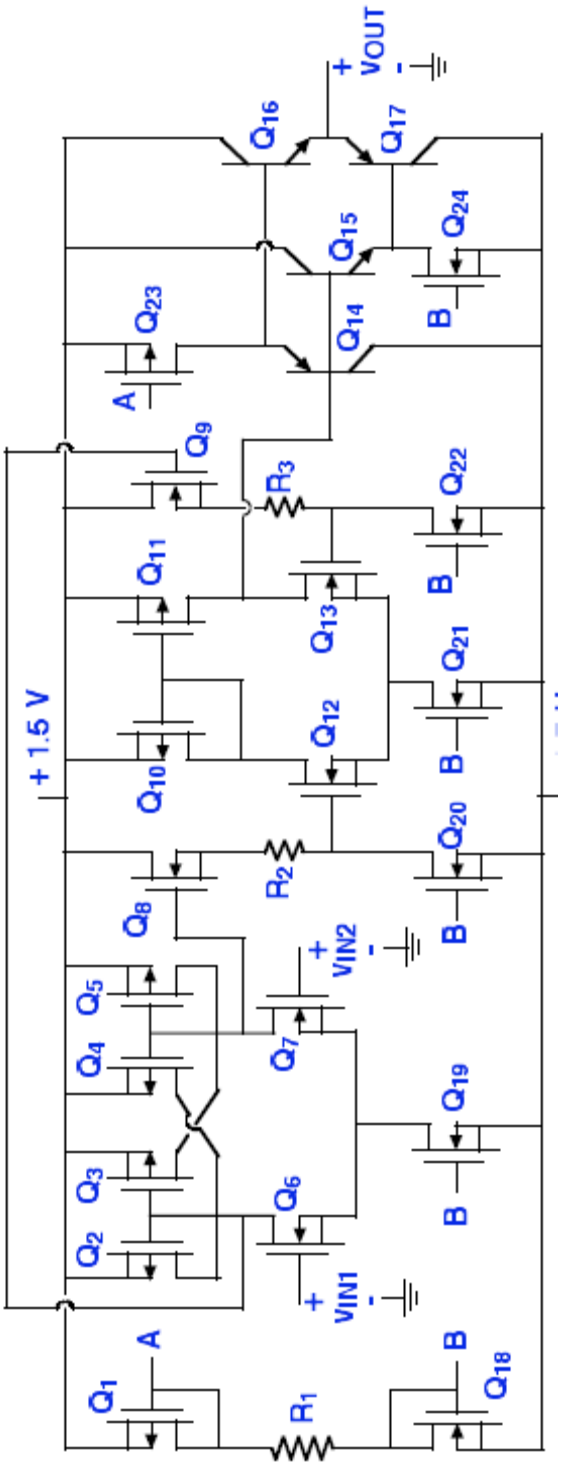

Fig. 1 High Gain BiCMOS Amplifier

Discussion of the Circuit

You should first look at the circuit carefully and identify its various pieces. Initially the circuit looks very complicated but if you break it into its component parts and understand what each does and how they interact, you will find that the amplifier is actually much less formidable.

Begin by identifying the biasing circuitry and the current sources, in this case the n-channel MOSFETs Q_{18},Q_{19},Q_{20},Q_{21},Q_{22}, and Q_{24}; the p-channel MOSFETs Q_1 and Q_{23}; and the resistor R_1. The chain formed by Q_1,R_1, and Q_{18} determines the reference voltages at points A and B. In this way, the transistor Q_{18} establishes the reference voltage on the gates of Q_{19},Q_{20},Q_{21},Q_{22}, and Q_{24}; and transistor Q_1 establishes the reference voltage on the gate of Q_{23}.

Once you see which transistors are involved in the biasing you can mentally replace them with current sources, as has been done in Figure 2, and ignore those devices until much later. Focus first on determining what bias currents you want from each current source, and the values of V_{GS} you want on Q_1 and Q_{18}. When these are known, then you will be able to complete the design of the devices in the current sources. The design of the Q_1-R_1-Q_{18} chain, for example, will be relatively easy after you have a target current level and
target V_{GS}'s on Q_1 and Q_{18}.
Move on next to look at the amplifier stages themselves, starting with the input stage, Q_6 and Q_7. This stage is an n-channel MOSFET differential common-source stage loaded with a Lee Load formed by the p-channel MOSFETs Q_2,Q_3, Q_4, and Q_5. The Lee Load was invented by Professor Tom Lee of Stanford. It looks incrementally like a very large resistor for differential-mode inputs, and like a very much smaller resistor for common mode inputs. The difference-mode voltage gain is thus very large and the common-mode voltage gain is less than one (i.e., it is not a gain, but an attenuation). Consequently using the Lee Load results in a gain stage with a very large common-mode rejection ratio.

The second stage is an n-channel MOSFET differential source-follower level-shift stage, Q_8 and Q_9. The quiescent voltage drop across resistors R_2 and R_3 shifts the bias level at the input of the next stage to a lower value so you will be able to bias its output near zero volts. The primary role of this stage is to provide this bias level shift. Notice, however, that it does introduce some attenuation of the signal because of the current divider effect of the resistors in series with the output resistance of the current sources biasing the stage.

The third stage is a second common-source gain stage, , Q_{12} and Q_{13}, this time with a current-mirror load, Q_{10} and Q_{11}. The biasing of this stage is important to meeting the output voltage swing specification. The current mirror does several things: First, it provides an active load which effectively applies the output of Q_{10} to the gate of Q_{11}, so that the output due to the difference-mode signal input to Q_{10} is added to the

output due to the difference-mode signal input to Q_{13}. Doing this converts the output from a double-ended (or differential) output to a single-ended output, and does so in such a manner that we obtain an additional factor of two in gain. Second, the output resistance of the current mirror looks different for common-mode and difference-mode signals, which helps reduce the common-mode voltage gain.

The output of the third stage is taken from the node joining the drains of Q_{11} and Q_{13}, and is what is termed a "high impedance" node. In practice the quiescent value of the voltage on this node this voltage is sensitive to differences in the transistors and process variations. This is a typical situation in high gain differential amplifiers and the issue is dealt with by using the amplifier with feedback that stabilizes the quiescent output voltage very near to zero volts. It is still important to design the circuit so that this output voltage would be as small as possible (within the other design constraints) if every transistor in the circuit met the design specifications exactly, but the actual quiescent value of zero Volts will be established by an external feedback circuit.

The fourth "stage" is a pair of emitter-follower stages, one that uses a pnp BJT and the other that uses an npn BJT. These followers are coupled to the fifth, and final stage, which is a complimentary output stage called a push-pull stage. This is basically an emitter-follower stage in which an npn transistor (Q_{16} in this circuit) drives the load (i.e., supplies current to the load resistor) when the output voltage goes above zero, and a pnp transistor (Q_{17}) turns on and drives the load when the voltage goes negative.

The quiescent current through Q_{16} and Q_{17} will be the quiescent current through Q_{14} and Q_{15} multiplied by the ratio of the areas of the two sets of devices. The sizes of these devices will be important design parameters. ***REMEMBER: Please change Bipolar devices to CMOS devices!!!!***

Taken together the last two stages give the amplifier a low output resistance. When you do you design problem analysis of the last stage (the push-pull) both pairs of transistors (the pair Q_{14} and Q_{16}, and the pair Q_{15} and Q_{17}) are on and their incremental equivalents are in parallel. When the output goes positive, however, the lower pair (Q_{15} and Q_{17}) soon turns off and the upper pair (Q_{14} and Q_{16}) turns more strongly on and dominates the contribution of this part of the circuit to the output resistance and to the loading on the second gain stage. When the output goes negative, the lower pair dominates and the upper pair turns off. Also assume a 100 W load, and remember that the design spec is that the quiescent output voltage is 0 V.

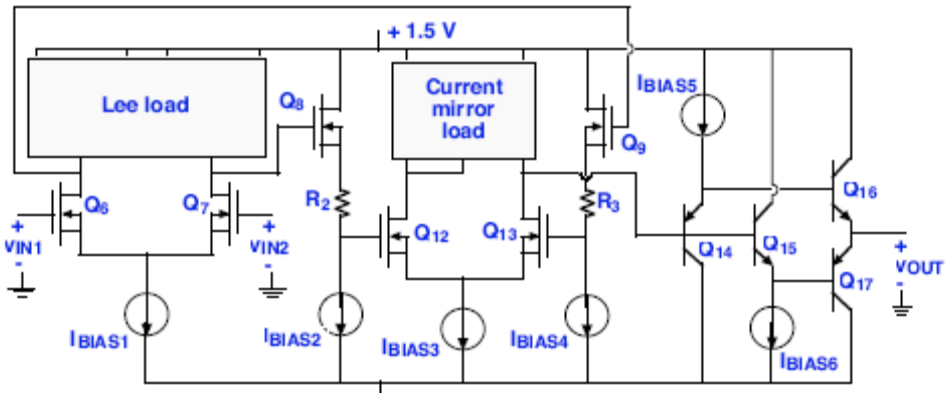

Figure 2 -A simplified schematic of the design