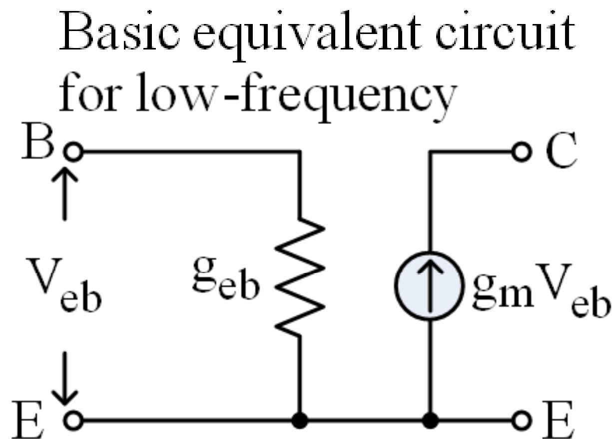
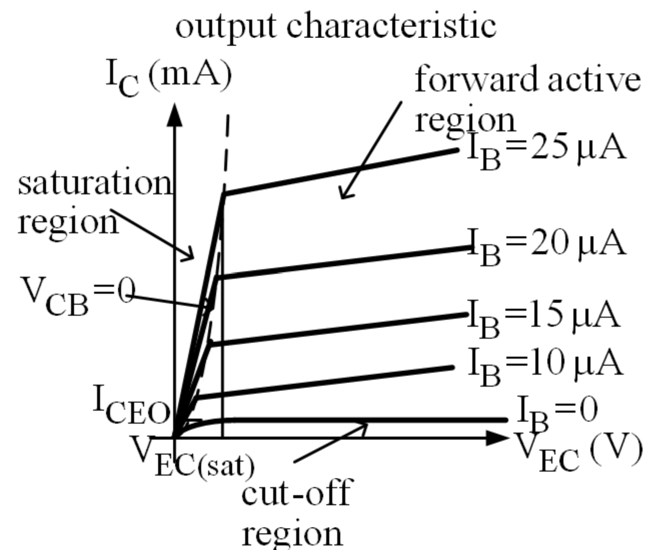
CLASS 10&11

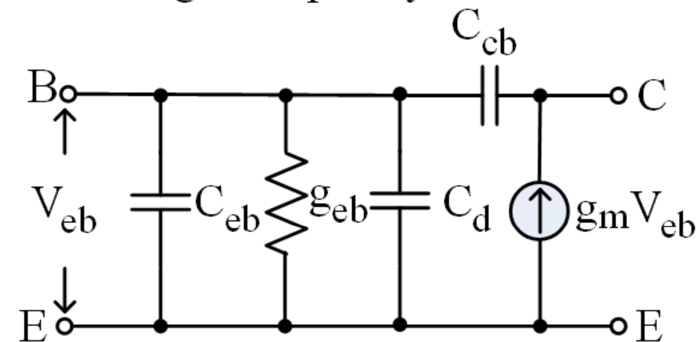
BJT small signal model and JFET

SMALL-SIGNAL EQUIVALENT CIRCUIT OF BJT





- **$g_m = I_c/V_{eb}$ is the transconductance.**
- **$g_{eb} = I_b/V_{eb}$ is the i/p conductance. This conductance must be included as we are considering the current that is flowing through the fb E-B junction.**
- **At higher frequencies, when E-B is fb, there exist a depletion capacitance, C_{eb}, and diffusion capacitance, C_d. For the rb B-C junction, there exist only the depletion capacitance, C_{cb}.**



<u>**Depletion capacitance:**</u>

Independent of whether the junction is forward or reverse biased, there exist the depletion region on both sides of the junction. The p-depletion region-n structure is similar to the structure of the capacitor. Due to the depletion region, depletion capacitance, C_j, exist.

$C_j = dQ/dV = dQ/(WdQ/\varepsilon A) = \varepsilon A/W$
(unit for C_j is F/cm^2)

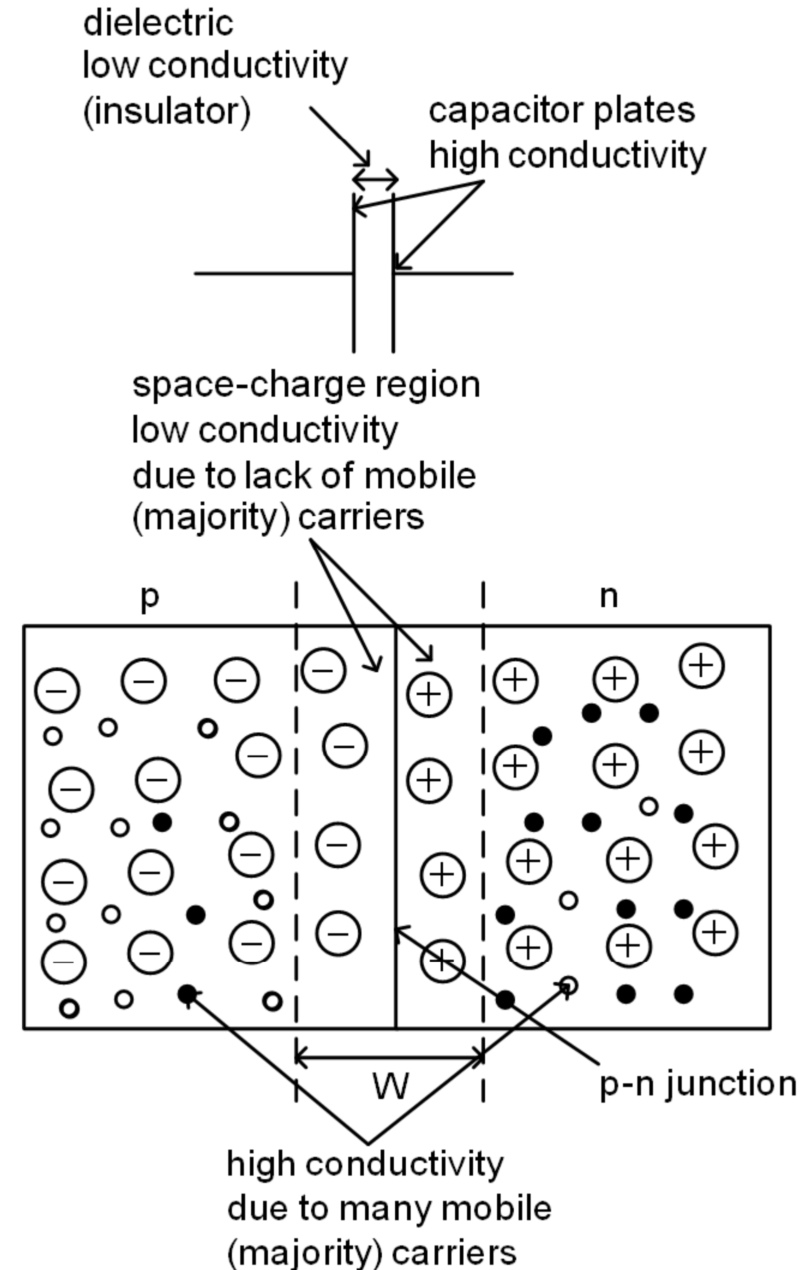
dQ = change of charge per unit area of the depletion layer.

dV = change of voltage applied.

A = cross-section area.

ε = permittivity of Si

W = width of the depletion region



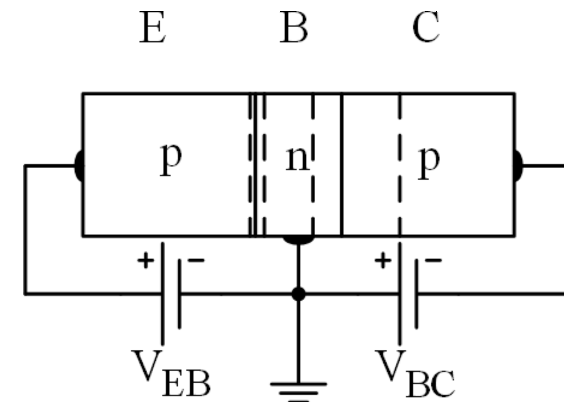
Diffusion capacitance

- **When the p-n junction is fb, large current flows through the junction. This will result in many mobile carriers to be in the neutral B. The change in the mobile carriers corresponding to the change in the biasing voltage will result in the diffusion capacitance, C_d.**
- **$C_d = (Aq^2L_p p_{no}/kT)e^{qV/(kT)}$**

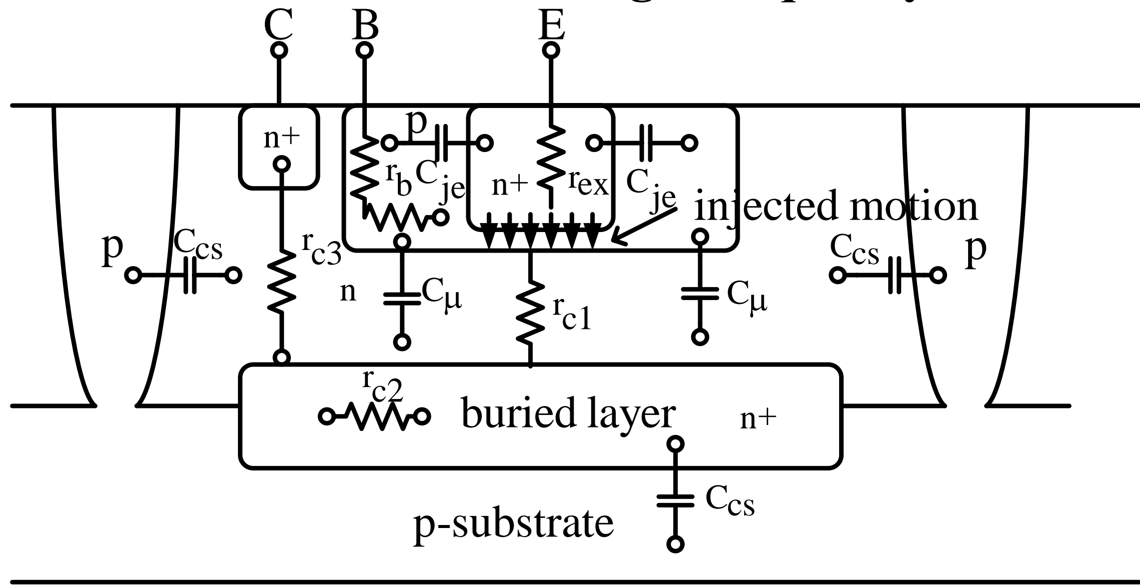
  where

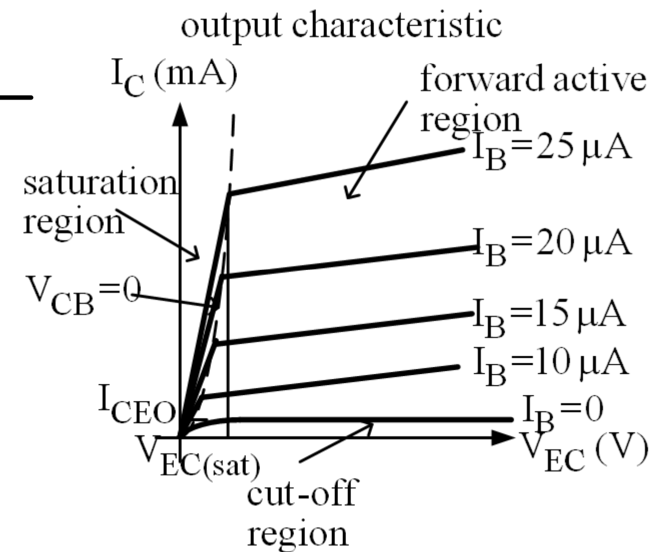
  L_p = diffusion length of hole in the n material

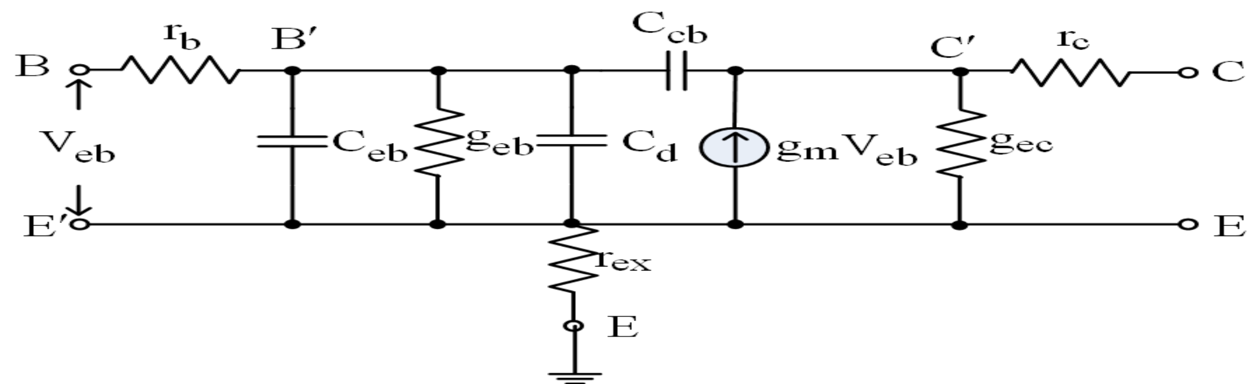
  p_{no} = equilibrium hole density in the n



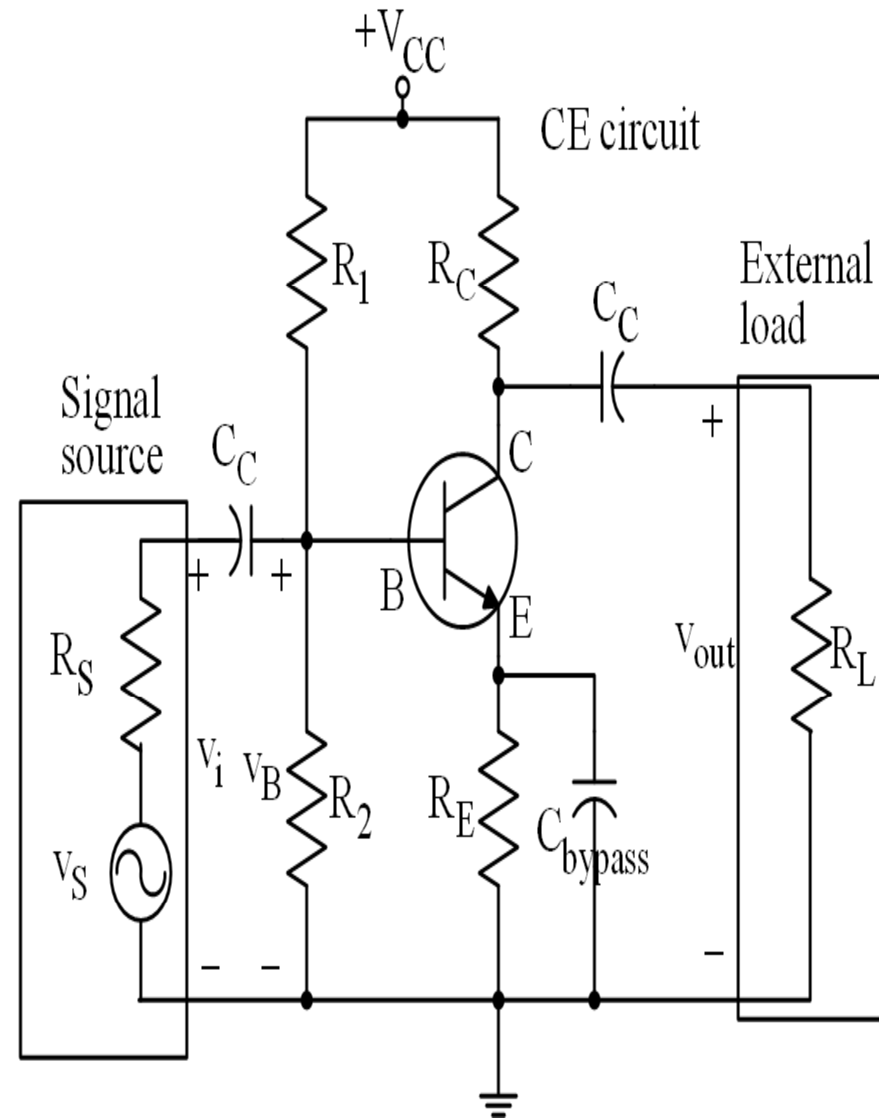
- **If the Early Effect (or base width modulation effect) is to be considered, the output conductance, $g_{ec} = I_c/V_{ce}$, has to be included.**
- **If the resistance of the B and C are to be included, the equivalent circuit of the BJT at high-frequency becomes:**



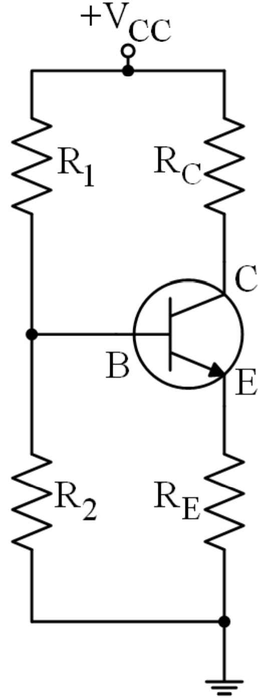




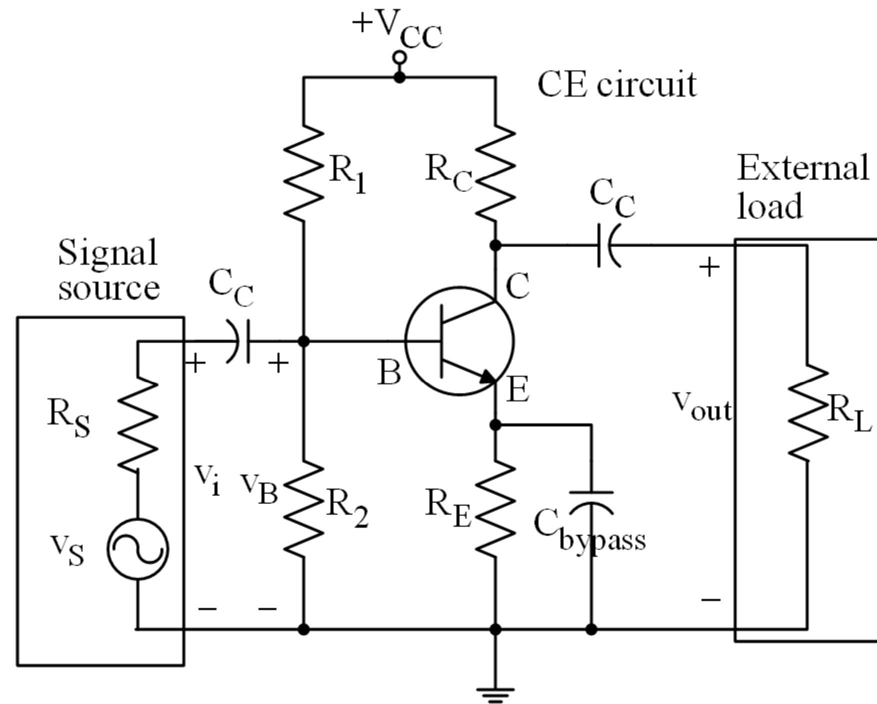
- **C_C is a coupling capacitor. It limits the DC signal to the transistor and the biasing circuit only. The DC signal cannot reach the signal source and the external load as capacitor to a DC is an open circuit [$X_C = 1/(2\pi fC)$].**
- **C_{bypass} is a bypass capacitor. It takes out R_E (the emitter resistor that can reduce the amplifier's gain) from the AC signal's path but let R_E plays its part in stabilizing the biasing of the transistor. To the AC signal, the capacitor is a short circuit.**



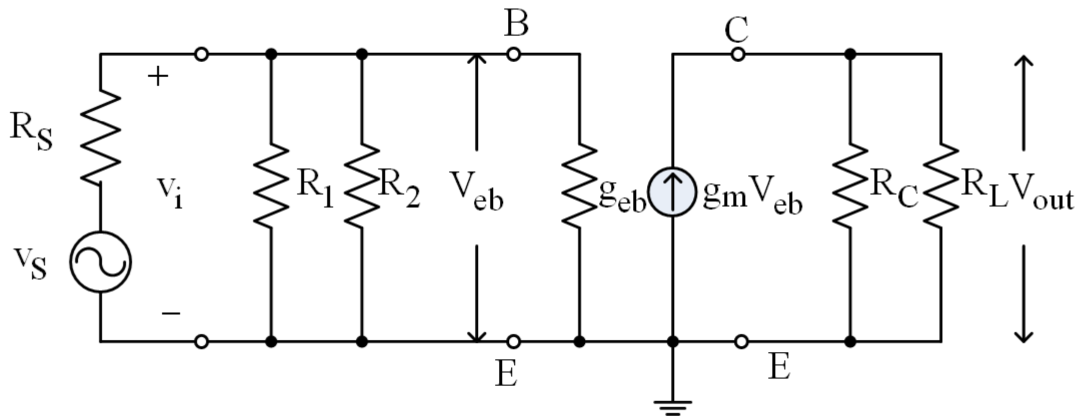
To analyze the biasing circuit (i.e. DC analysis),



CE Amplifier circuit



To perform AC analysis,



Field Effect Transistors (FET) and Bipolar Junction Transistors (BJT) Differences

	BJT	FET
1.	**Bipolar device** Both current carriers (electrons and holes) contribute to the current flow.	**Unipolar device** One current carrier (majority carrier) influences the current flow.
2.	**Current controlled device** Base current (I_B) controls Collector current (I_C).	**Voltage controlled device** Gate to Source voltage (V_{GS}) controls the amount of current (I_D) flowing.
3.	**Z_i of BJTs < Z_i of FETs** Depending on the configuration: CE - A_V is high, Z_i is quite high. CC - A_V is 1, Z_i is high. CB - A_V is high, Z_i is low.	**High input impedance** Z_i = hundreds of MΩ.
4.	**Not as stable** as the FET towards temperature variation.	More **stable** towards temperature variation.
5.	**Larger and more complex** than FET.	**Smaller in size and easier to fabricate** as compared to the BJT.

Due to 4 and 5, FET can be found in many digital ICs.

FIELD EFFECT TRANSISTORS

1. **Junction Field Effect Transistor (JFET)**
2. **Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET)**

<u>Generally known as:</u>

1. **Metal-Insulator-Semiconductor FET (MISFET) where the insulator may not be silicon dioxide (SiO_2) and semiconductor may not be Silicon (Si).**
2. **Insulated Gate FET (IGFET) symbolizing the device which Gate is insulated from the Body by the SiO_2.**

The insulated Gate from Body causes the gate current (I_G) to be considered as 0 in many analysis and calculation. In reality, this current is in the femto (10^{-15}A) range.

Differences between JFET and MOSFET

- **The Gate of the MOSFET is insulated from the channel (and Body) by a layer of SiO_2.**
- **MOSFET does not have a p-n junction that controls the width of the channel and consequently the current.**

MOSFET Application

- **In Very-Large-Scale-Integrated (VLSI) circuits. Examples: microprocessor and memory chips.**
- **At present, even the RF analog integrated circuits are implementing MOSFETs as these devices have smaller dimensions and cheaper to fabricate.**

  To summarize, the MOSFETs are typically used in IC design.

Types of MOSFET

- **Depletion-enhancement (typically known as DE-MOSFET)**
- **Enhancement-only MOSFET (typically known as E-MOSFET)**

JUNCTION FIELD EFFECT TRANSISTOR (JFET)

2 Types:

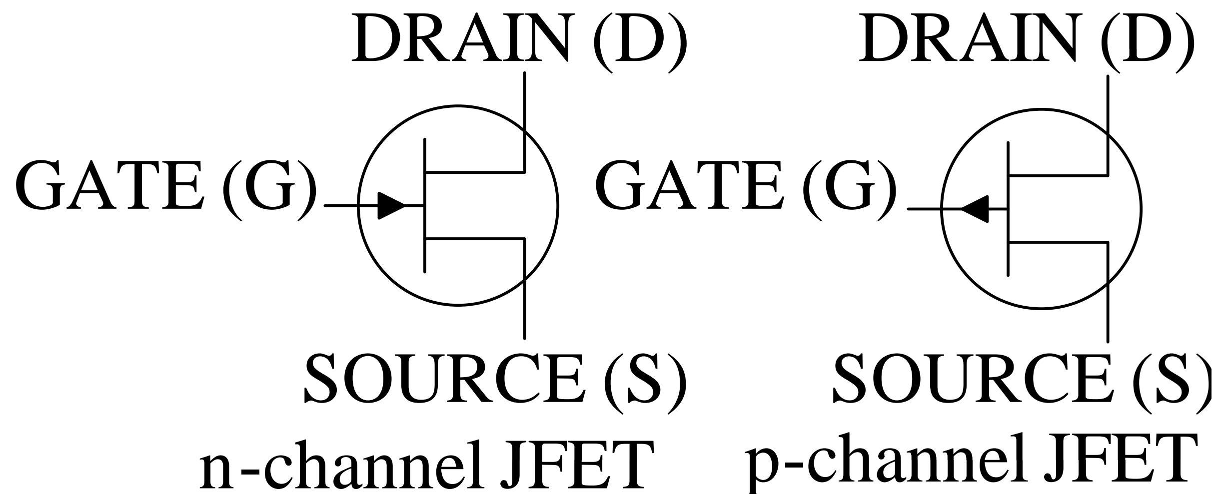
1. **n-channel JFET**

   The current carriers in an n-channel JFET are the electrons.

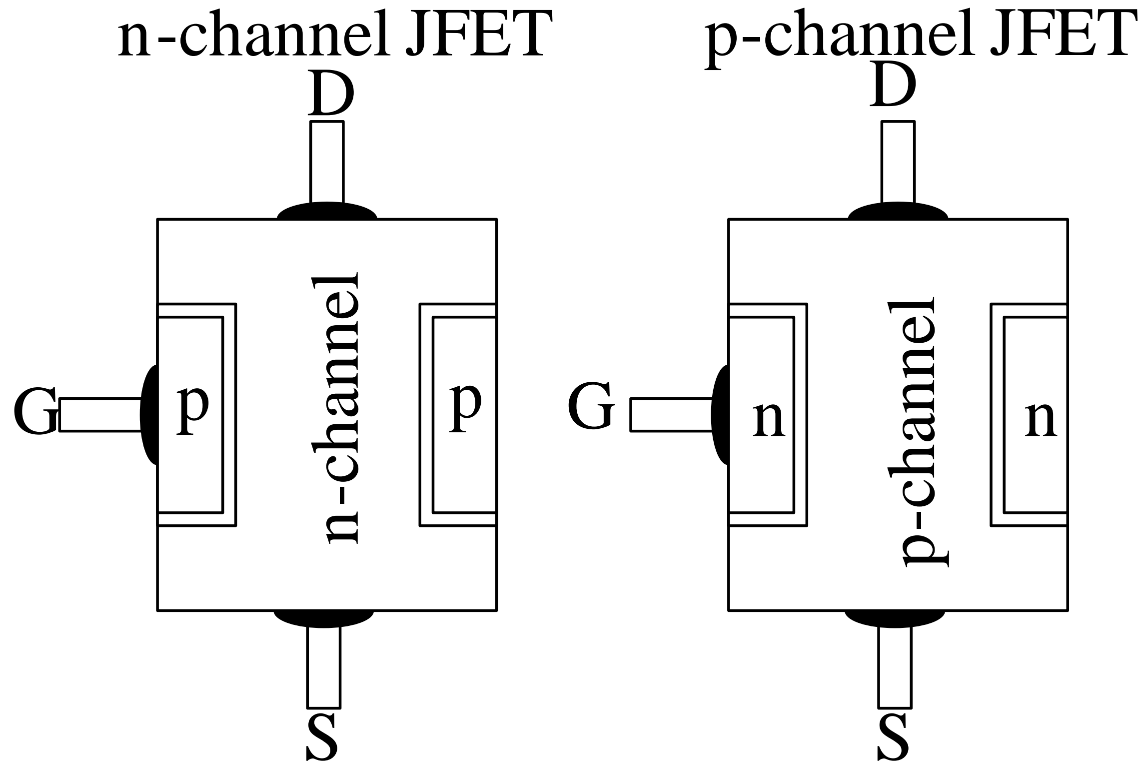
2. **p-channel JFET**

   The current carriers in a p-channel JFET are the holes.

Symbols:



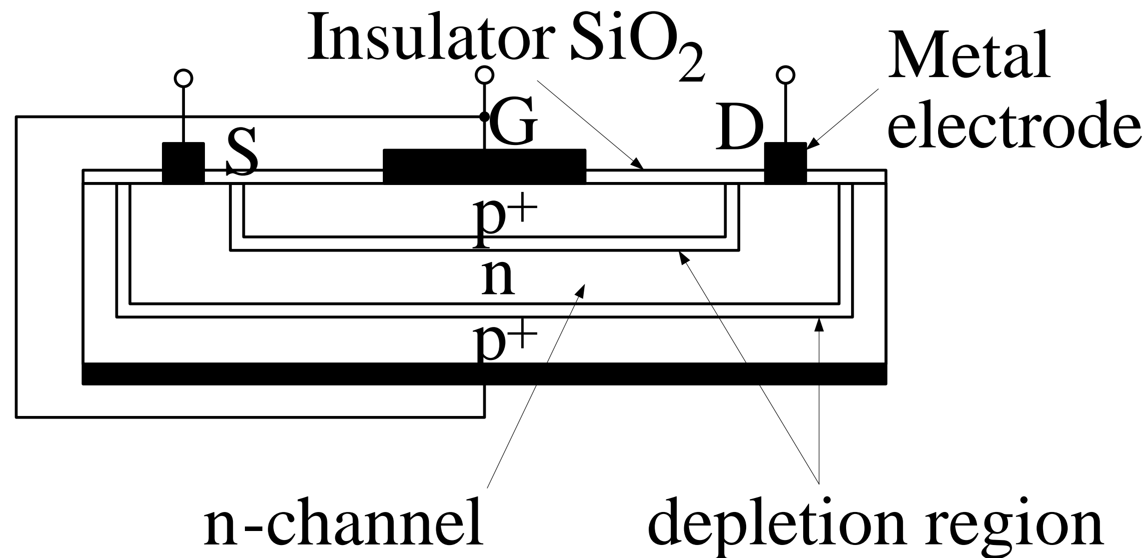
Simplified cross-section of a JFET



Both the p regions in the n-channel JFET and the n regions in the p-channel JFET are electrically connected.

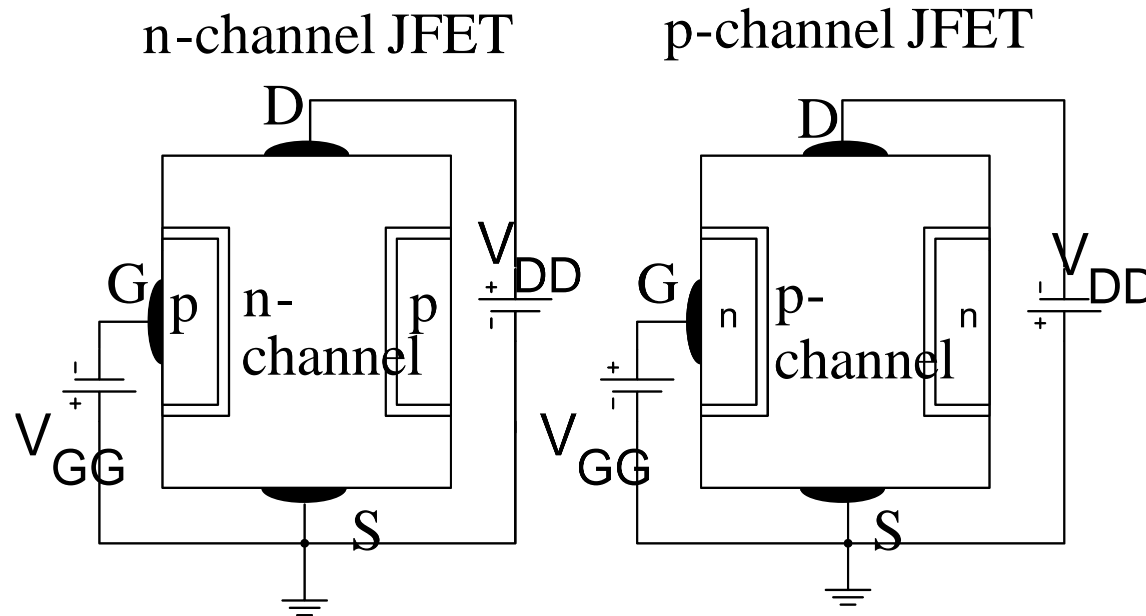
A more practical cross-section of an n-channel JFET

Both the p^+ regions in the n-channel JFET are electrically connected.



Basic operation of a JFET

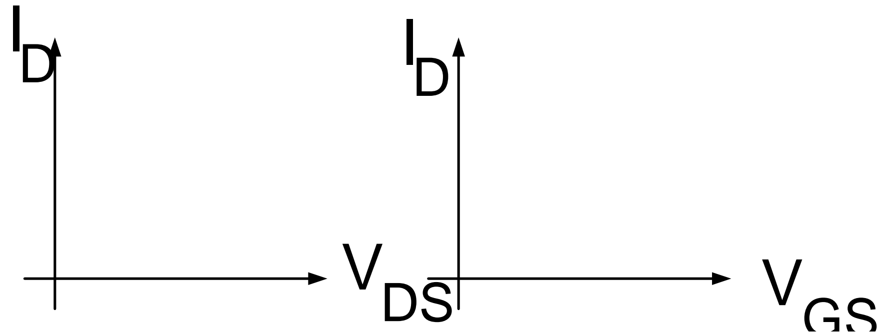
- As an amplifier. The condition that enables the JFET to operate as an amplifier is the G-S that has to be reverse biased.
- V_{DD} is to provide the difference in potential between D-S to enable the majority current carrier to move from S to D.
- V_{GG} is to reverse bias the G-S.

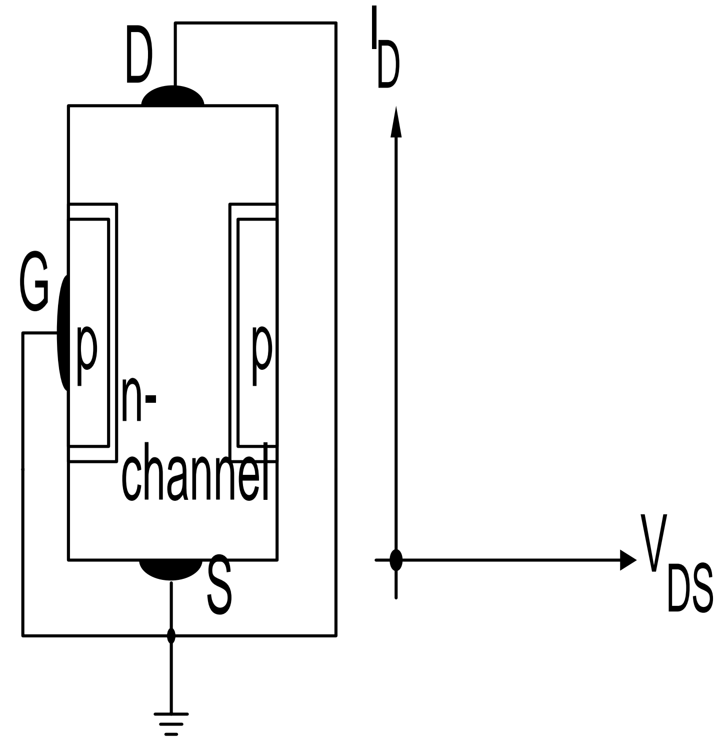


JFET Characteristics

1. Drain characteristic
2. Transfer characteristic

Drain characteristic | **Transfer characteristic**





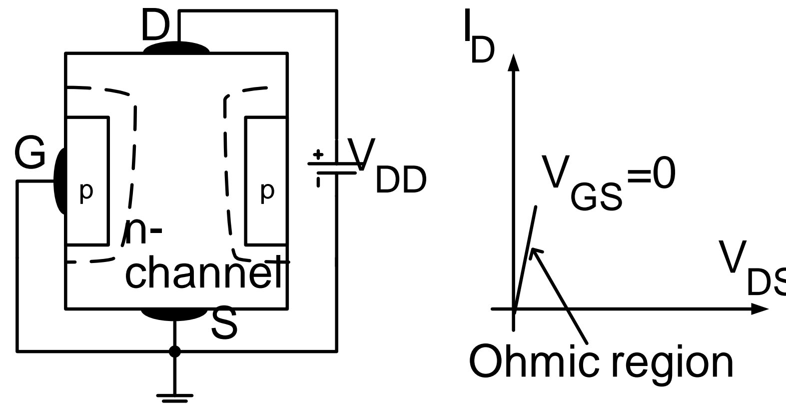
Drain Characteristic

1. $V_{GS} = 0$ and $V_{DS} = 0$

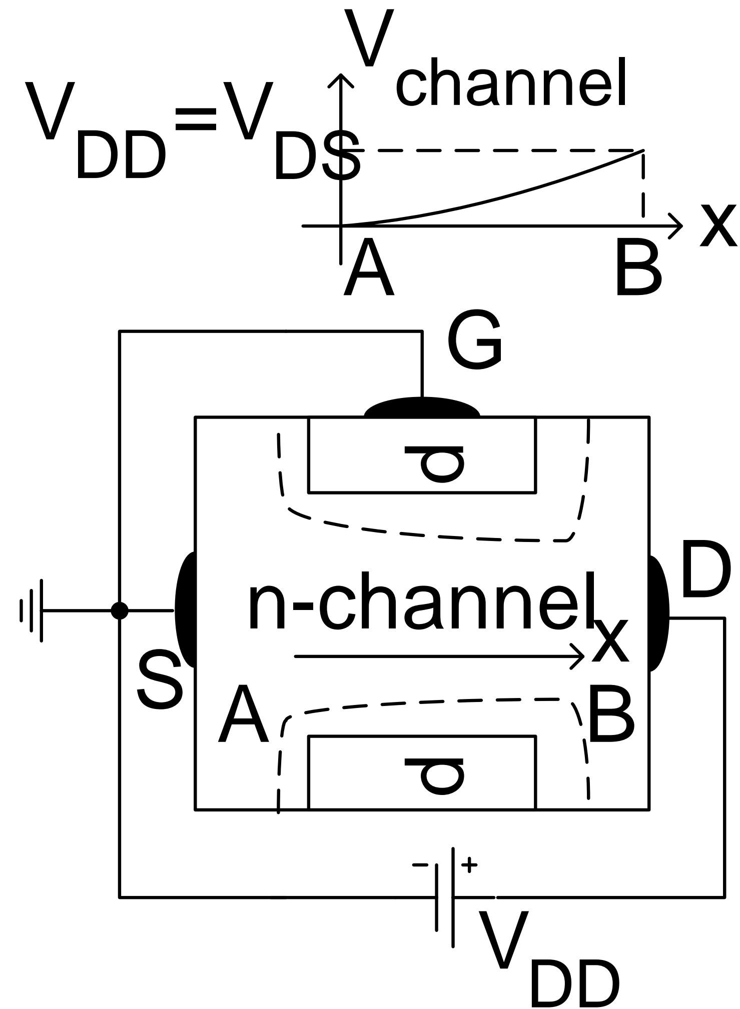
   No difference in potential between D and S. No majority carriers flowing from S to D. Hence, $I_D = 0$.

2. V_{GS} = 0 and V_{DS} is small.

- **$V_{DS} = V_D - V_S = V_{DD} - 0 = V_{DD}$**
- **$V_{GS} = V_G - V_S = 0$**
- **G–S is reverse biased.**
- **Depletion regions exist.**
- **V_D is positive. Therefore, G-D is reverse biased. Again, depletion region exists.**
- **Comparing G-D and G-S, G-D is more reverse biased. Hence, the depletion region grows wider towards D.**
- **For a small V_{DS}, the size of the G-D depletion region does not affect the width of the channel significantly. Under this condition, the depletion region does not influence the current. When V_{DS} increases, I_D will also increase. The I_D versus V_{DS} characteristic is linear. Under this condition, $V_{DS} = I_D R$ and the n-channel is a basically a resistance. Hence, this region of the drain characteristic is known as the ohmic region.**

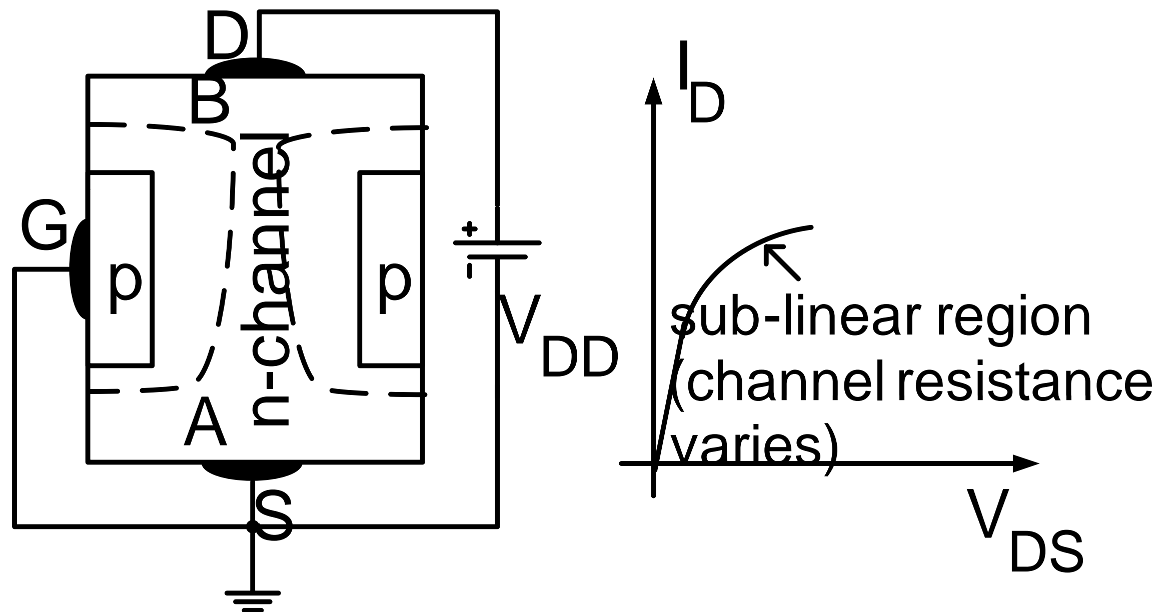


There is a voltage drop along the channel from A to B. $V_A = V_S = 0$ and $V_B = V_D = V_{DD}$. The voltage becomes more positive towards B. Hence, the p-n junction from G to channel becomes more reverse biased from A to B.



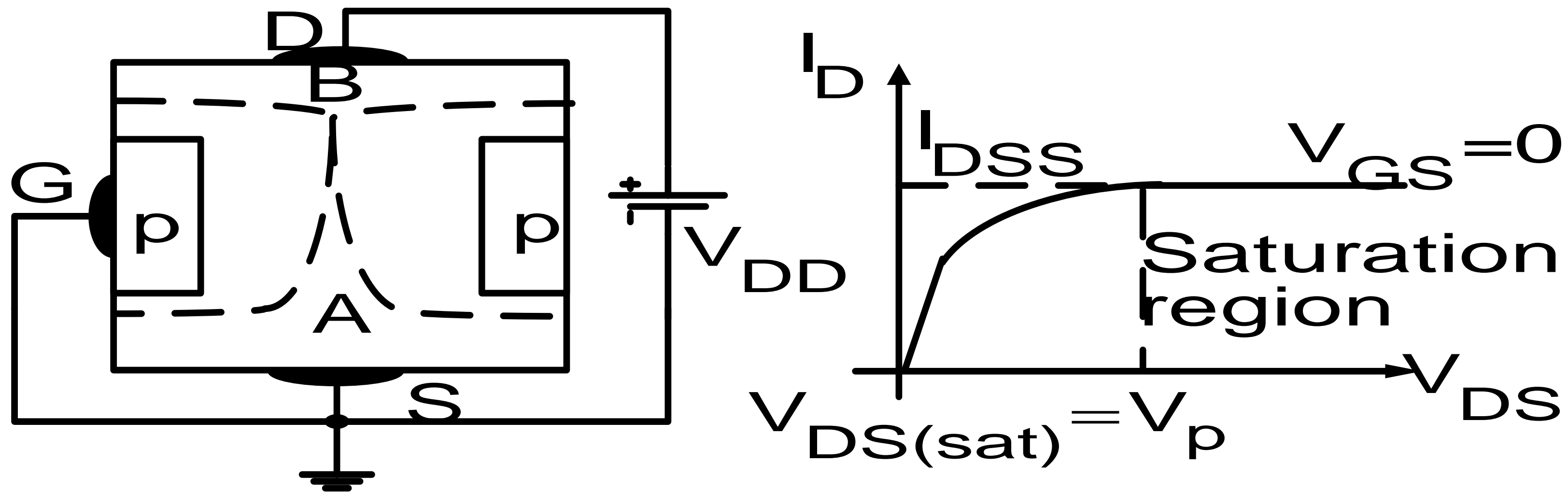
3. $V_{GS} = 0$ and V_{DS} is increased.

When V_{DS} increases, the G to channel p-n junction becomes more reverse-biased near D. Depletion region becomes wider and channel becomes narrower near D. The channel is basically a resistor and the effective channel resistance increases when depletion region widens. R_{AB} increases with the increment of V_{DS}. $R_{AB} = \Delta V_{DS} / \Delta I_D$. I_D does not increase linearly with V_{DS} anymore. In the sub-linear region, slope decreases and resistance increases.



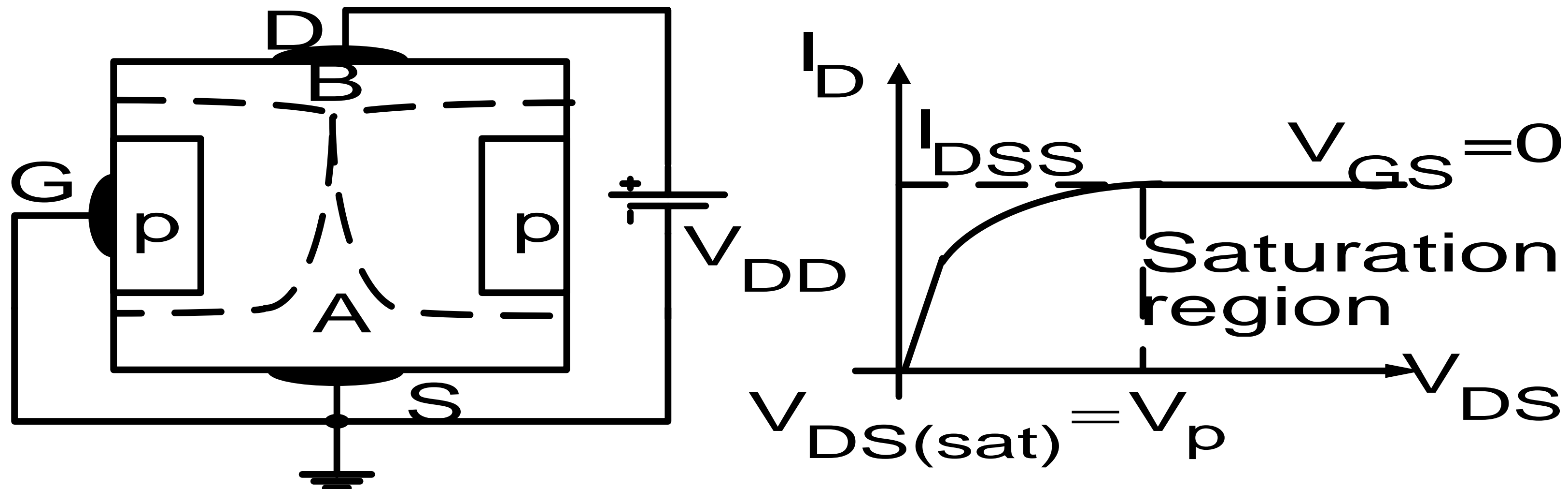
4. $V_{GS} = 0$ and V_{DS} is further increased.

- The reverse biasing of the G to D p-n junction is enough to make the depletion regions meet near D. The channel is said to be pinched-off. Any further increment to the V_{DS} will no longer increase the I_D.
- At pinched-off, $V_{DS} = V_{DS(sat)}$.
- $V_{DS(sat)}$ = the voltage across D-S when pinched-off occurs.
- For $V_{DS} > V_{DS(sat)}$, I_D is fixed. Transistor is in the saturation region and I_D is independent of V_{DS}.
- When $V_{GS} = 0$, $V_{DS(sat)} = V_p$ and $I_D = I_{DSS}$ for $V_{DS} \geq V_{DS(sat)}$.



- **$I = Js = neU_D s$ where J is the current density, s is the cross section area of the channel, U_D is the carrier drift velocity, e is the electronic charge and n is the carrier concentration. For an n-channel JFET, $I = N_D e U_D s$ where N_D is the electron concentration ≈ donor dopant concentration.**

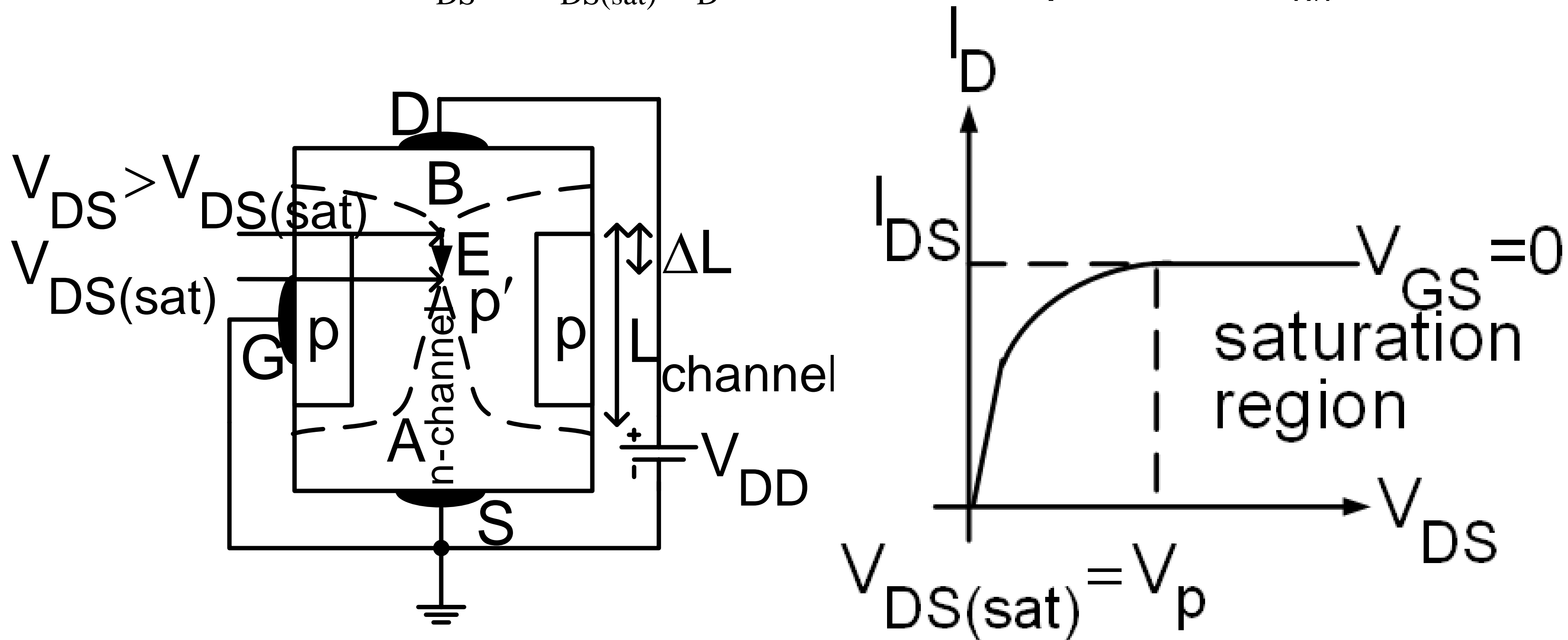
- **When approaching pinched-off, s becomes very small and U_D has to become very large to maintain the current flow. The current density $J = N_D e U_D$ becomes very high and under this condition, the drift velocity U_D is at its maximum.**



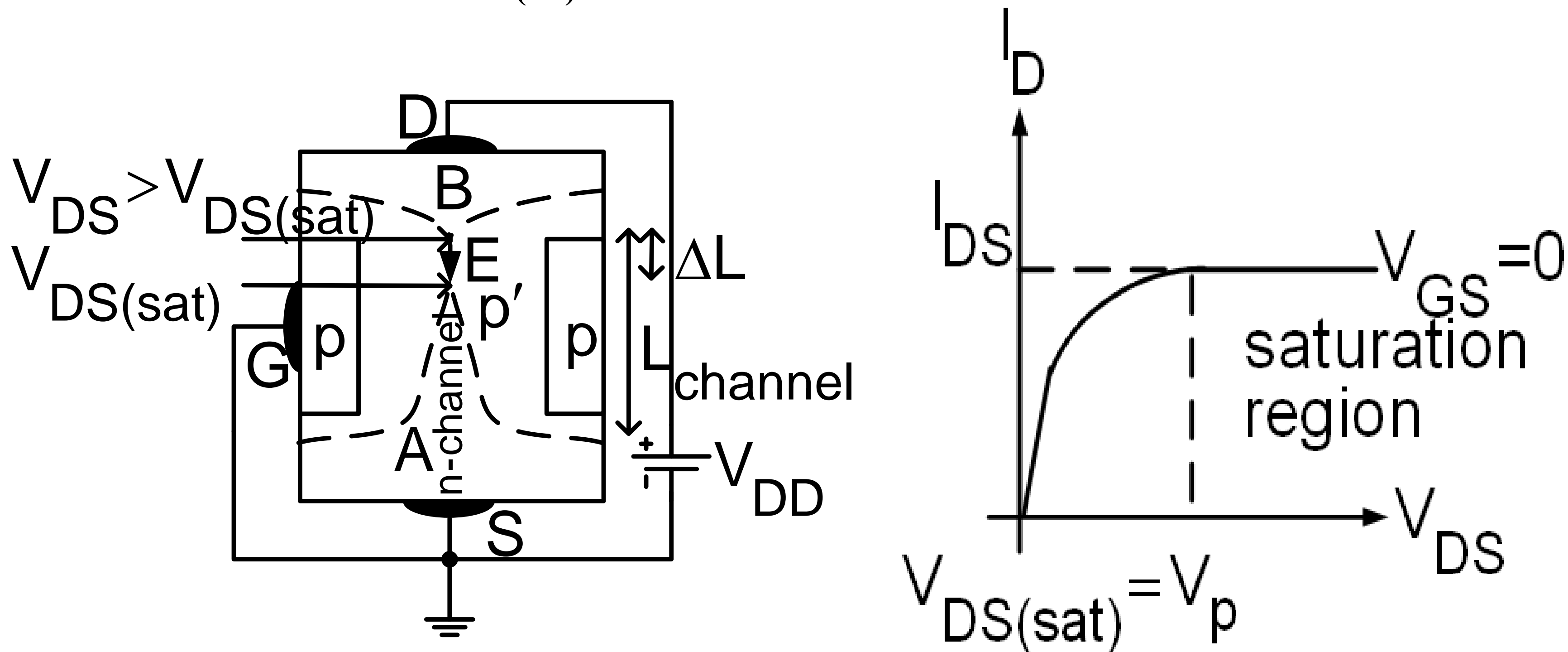
5. $V_{GS} = 0$ and $V_{DS} > V_{DS(sat)}$.

E is the electric field. The n-channel is separated from D by a space charge region that has a length of ΔL. From S, the electrons move along the channel, got injected into the space charge region, and subsequently being swept by E to move to D.

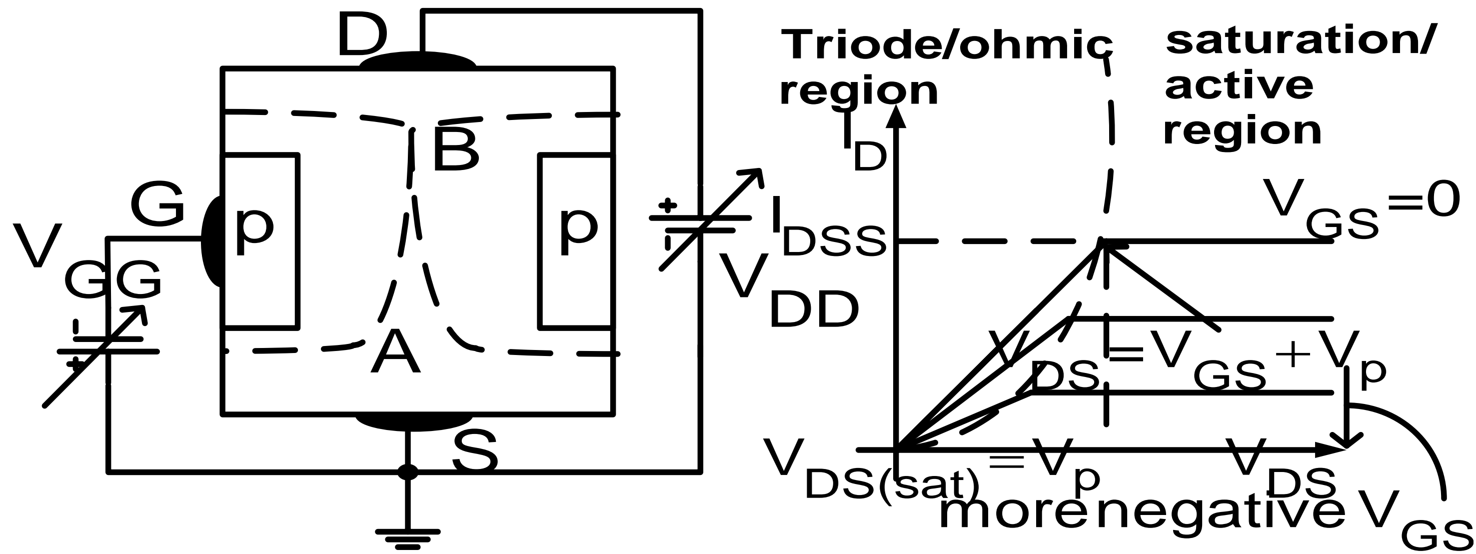
If $\Delta L \ll L_{channel}$, the electric field in the n-channel does not change from the one when $V_{DS} = V_{DS(sat)}$. I_D is fixed and independent of V_{DS}.



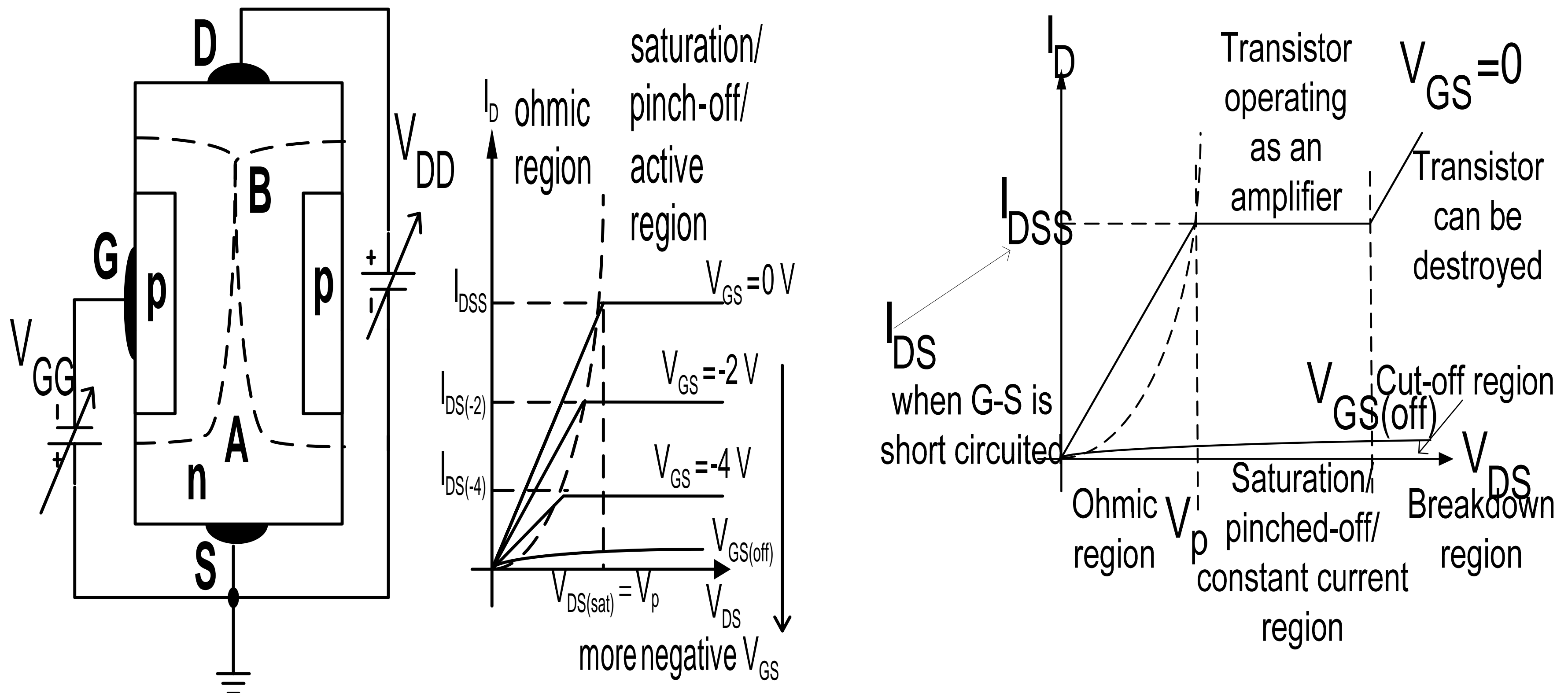
- I_D **is determined by the channel resistance from A to p', and not by the pinched-off part of the channel. When** $V_{DS} > V_{DS(sat)}$**, the excess voltage i.e.** $V_{DS} - V_{DS(sat)}$**, is across** ΔL **as this part is depleted of carriers and consequently has high resistivity.**
- **p' has a voltage** $V_{DS(sat)} = V_p$ **as this is the potential that causes the depletion regions to meet.** $I_D = V_{DS(sat)} / R_{Ap'}$**. If** $\Delta L << L_{channel}$**, then** $I_D = V_{DS(sat)} / R_{Ap'}$ **is equivalent to** $V_{DS(sat)} / R_{AB}$ **when** $V_{DS} = V_{DS(sat)}$**. Hence, although** $V_{DS} > V_{DS(sat)}$**,** I_D **remains unchanged.**



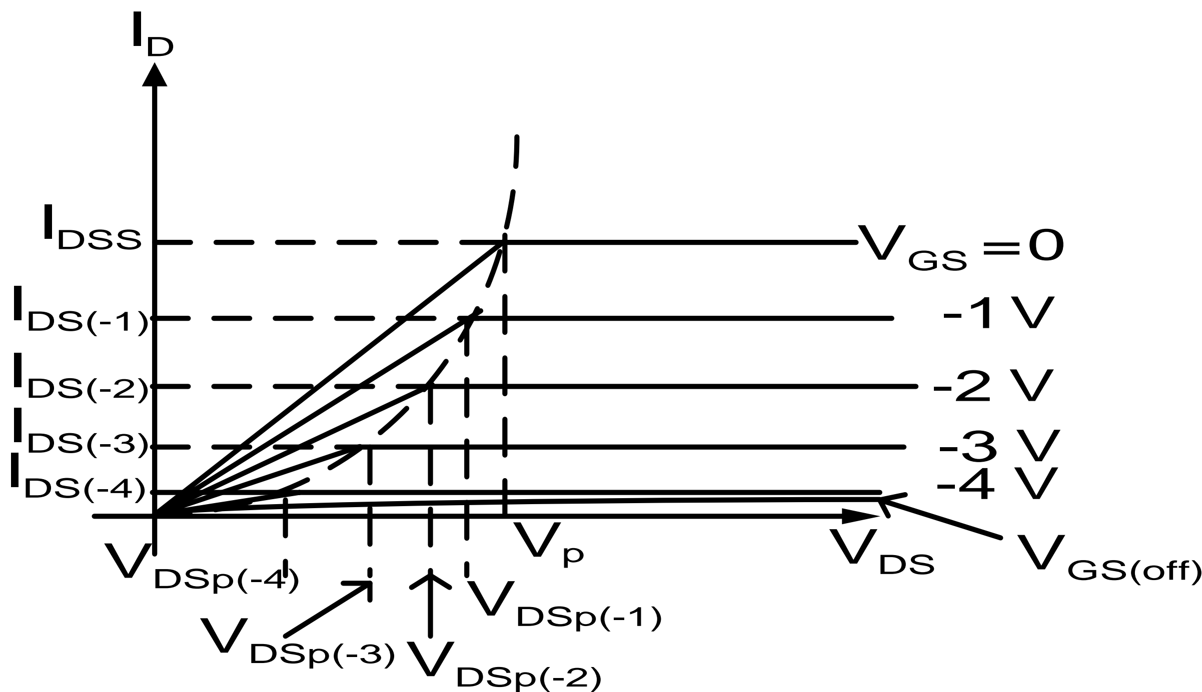
- **If the magnitude of V_{GG} (V_{GS}) increases, V_G becomes more negative and the G-S becomes more reverse biased. Hence, a smaller V_{DS} is required to achieve pinched-off and the I_D at saturation will be smaller than I_{DSS}.**
- **To operate a JFET as an amplifier, the JFET has to be biased in the saturation region. This means that $V_{DS} \geq V_{GS} + V_p$. The triode region is for $V_{DS} \leq V_{GS} + V_p$. At pinch-off, $V_{DS(sat)} = V_{GS} + V_p$. Hence, if V_{GS} is more negative, $V_{DS(sat)}$ becomes smaller. (John Seymour, "Electronic Devices and Components, Second Edition, 1988, Longman)**
- **V_p and I_{DSS} are the JFET parameters and specified in the data sheet.**

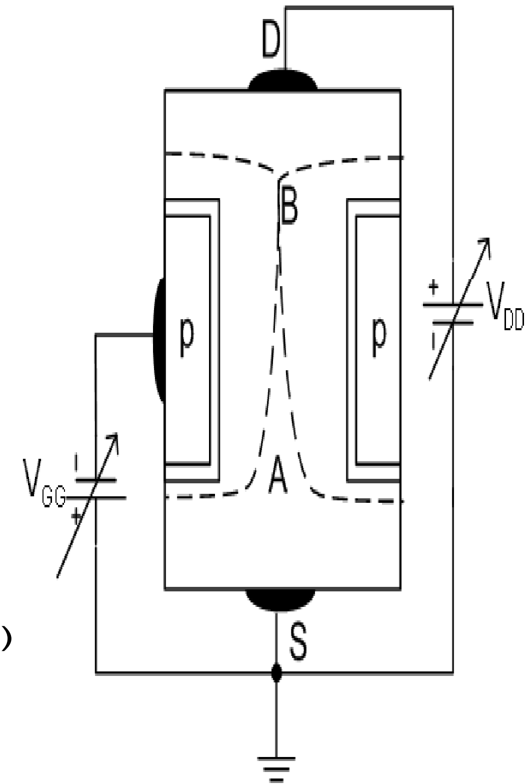


- **From the drain characteristic, as V_{GS} becomes more negative, the saturated current, I_{DS}, becomes smaller. When the V_{GS} is negative enough (i.e. when $V_{GS} = V_{GS(off)}$), $I_D \approx 0$. This condition occurs as when $V_{GS} = V_{GS(off)}$, the depletion region becomes large enough that it closes the channel. $V_{GS(off)} = - V_p$**



- The family of drain characteristic curves shows that when V_{GS} becomes more negative, V_{DSp} (or $V_{DS(sat)}$) and I_{DS} become smaller.
- I_D is dependent on the width of the channel. The width of the channel is dependent on the depletion region. The depletion region is dependent on the V_{GS}. Hence, V_{GS} is controlling the value of I_D. This is the reason why the JFET is known as a voltage controlled device.
- Pinched-off occurs when $V_{DS} = V_{DS(sat)}$.

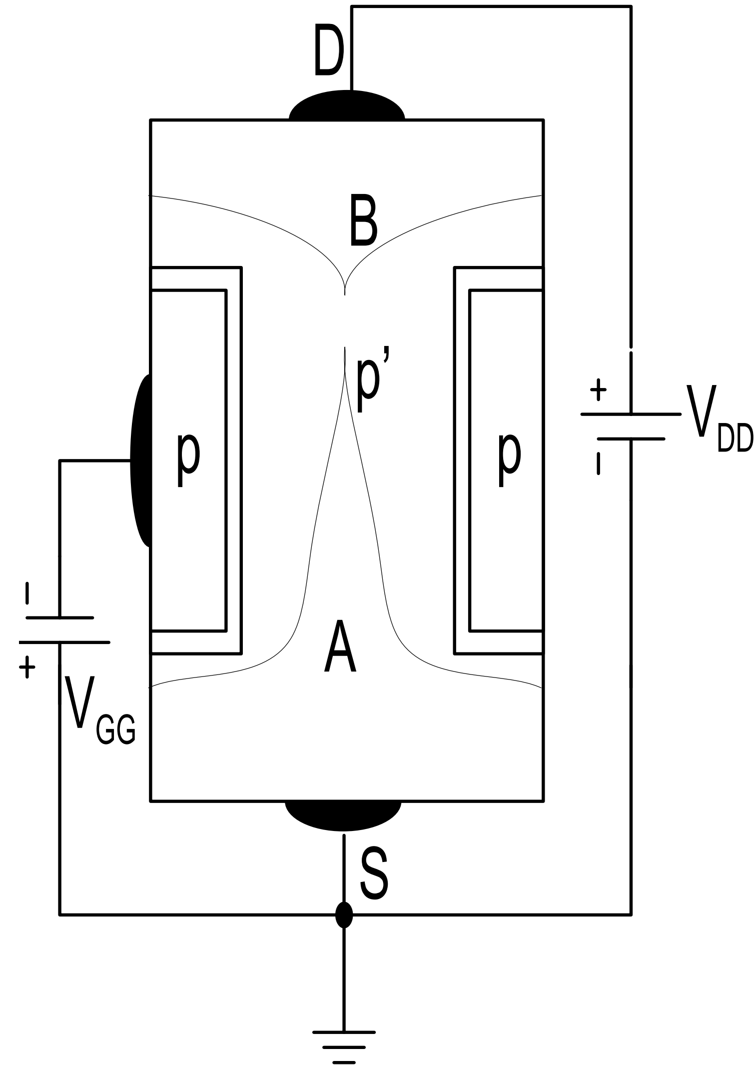




- **During pinch-off:**

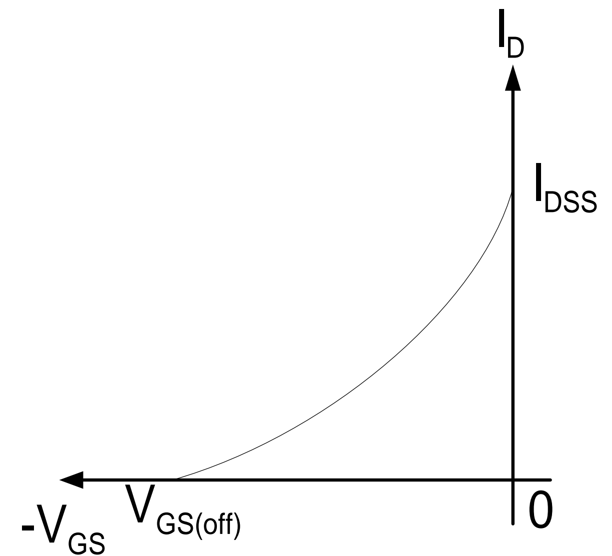
$$I_{DS} = \frac{V_{DS(sat)}}{R_{Ap'(V_{GS})}} = \frac{V_{GS} + V_p}{R_{Ap'(V_{GS})}}$$

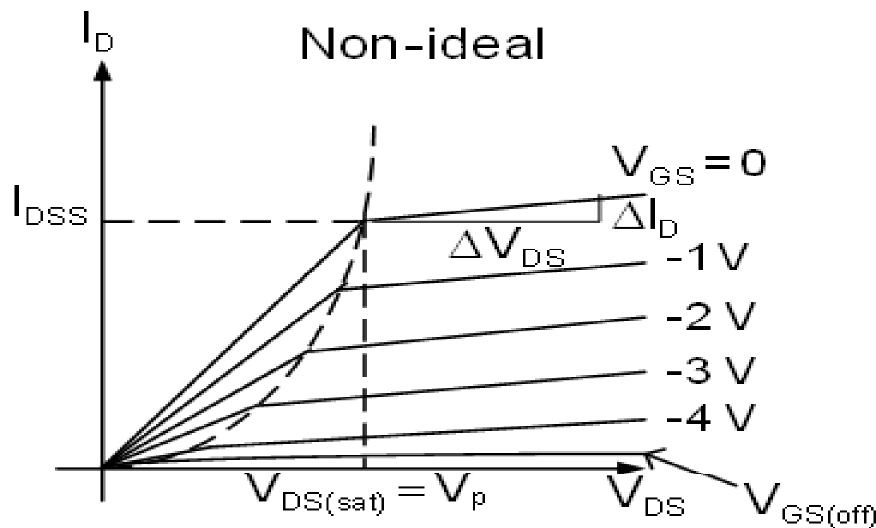
- **When V_{GS} becomes more negative, $V_{DS(sat)}$ reduces and $R_{Ap'(V_{GS})}$ increases. $R_{Ap'(V_{GS})}$ increases as the depletion region increases. Hence, I_{DS} decreases.**

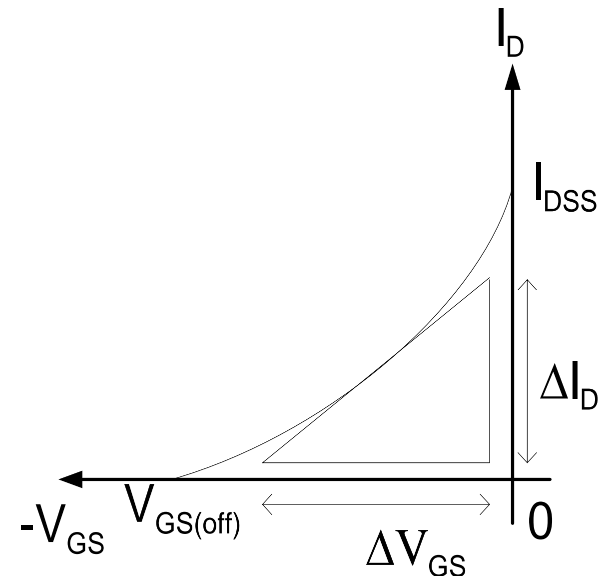


TRANSFER CHARACTERISTIC

- $I_D = I_{DSS}$ when $V_{GS}=0$ and $I_D = 0$ when $V_{GS}=V_{GS(off)} =-V_{p.}$
- I_{DSS} and $V_{GS(off)}$ are the JFET parameters which are available in the JFET data sheet.
- Another important JFET parameter is the forward transconductance, g_m.
- $g_m = \Delta I_D / \Delta V_{GS}$ at a fixed V_{DS} and the V_{DS} has to be in the saturation/fixed-current/pinch-off region.



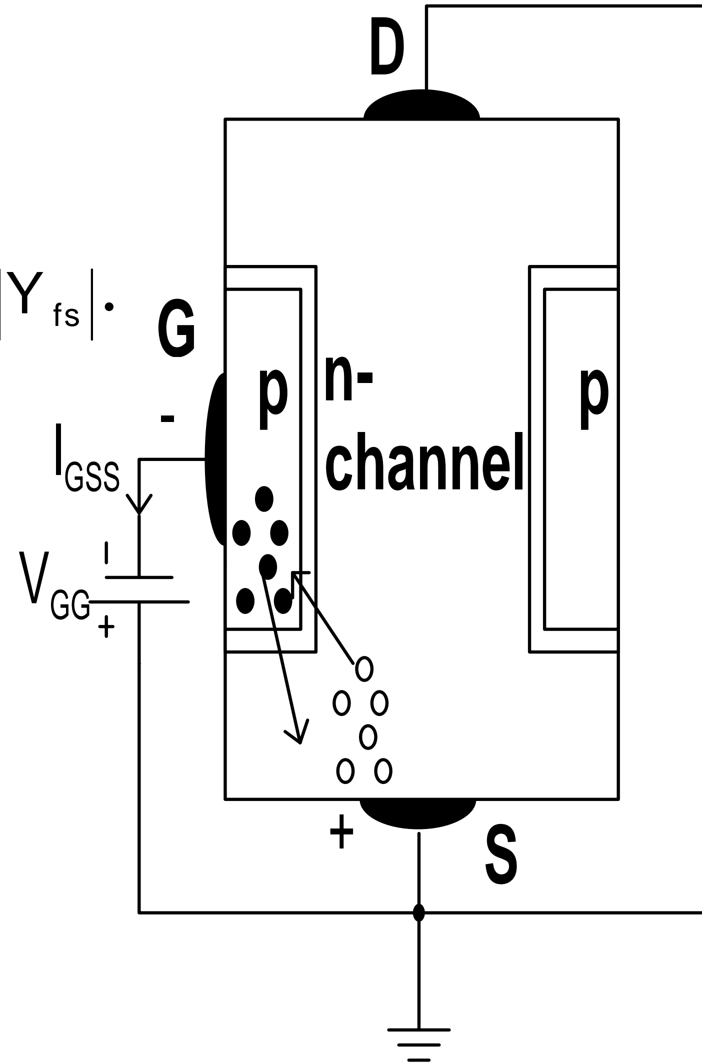




- g_m at $V_{GS} = 0$ is known as g_{m0}.
- $g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]$
- $g_{m0} = \frac{2I_{DSS}}{|V_{GS(off)}|}$
- In the data sheet g_{m0} is represented by $|Y_{fs}|$.

Important parameters of the JFET

1. R_{IN}



Besides $V_{GS(off)}$, I_{DSS} and g_{m0}, another parameter of the JFET is R_{IN}.

$$R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$$

- I_{GSS} is the G-S current when the D-S is short circuited. I_{GSS} is given in the data sheet. Since I_{GSS} is from the flow of minority carriers, I_{GSS} increases with the increment of temperature, T, at a fixed V_{GS}. I_{GSS} is the G reverse current at a known V_{GS}. As I_{GSS} increases with T, R_{IN} will be reduced as $R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$.
- The value of I_{GSS} is very small making the value of R_{IN} to be very large. Hence, the input impedance, Z_i, is very large.