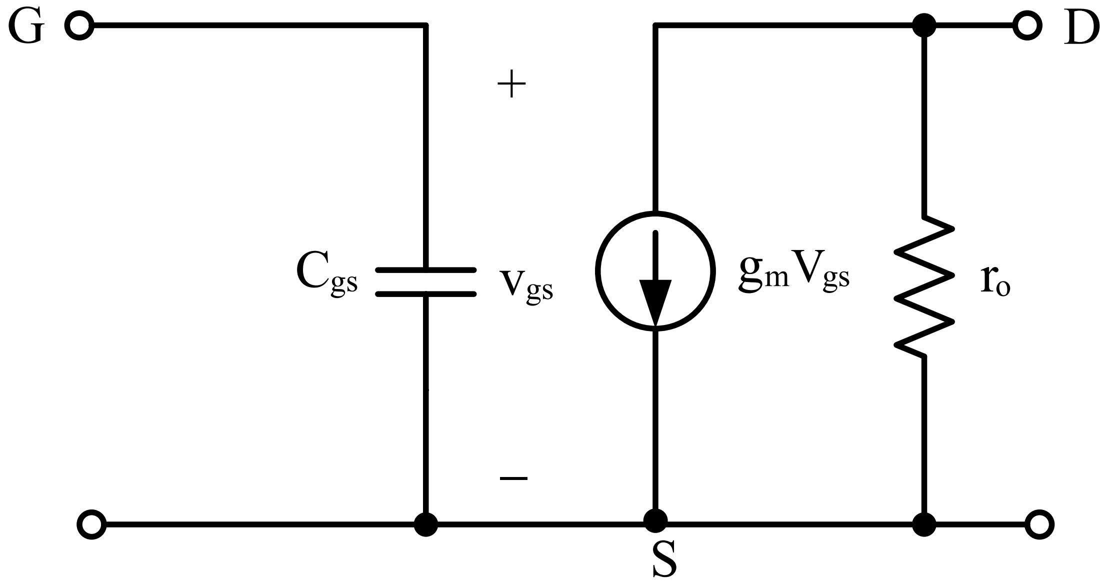
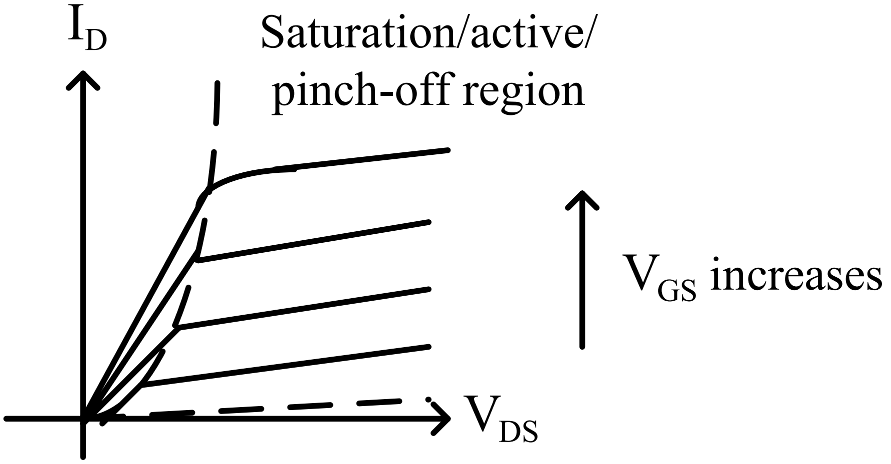
1.6.5 Basic small-signal model of the MOS transistor



This model is for the transistor in the sat/active region. This model is called the hybrid-π model.

1.6.6 Body transconductance

I_D is a function of both V_{GS} and V_{BS}. V_{GS} controls the vertical electric field which controls the channel conductivity and, hence, I_D. V_{BS} changes the threshold, which changes I_D when V_{GS} is fixed. This effect resulted from the influence of the substrate acting as a second gate and is called the body effect. The body of a MOSFET is usually connected to a constant power supply voltage which is a small signal or ac ground.



Output characteristic of NMOS

In the sat./active region, the V_{DS} has no influence on the I_D (if the channel modulation effect is not considered). The I_D is influenced only by the V_{GS}. V_{GS} ↑ I_D ↑. However, when $V_{SB} \neq 0$, V_t will change correspondingly. I_D will change too. Hence, the term "second gate" for the substrate if body effect is considered.

$$I_D = \frac{k'}{2}\frac{W}{L}\left(V_{GS} - V_t\right)^2\left(1 + \lambda V_{DS}\right) \qquad (1.157)$$

The transconductance from the body or second gate:

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = -k'\frac{W}{L}\left(V_{GS} - V_t\right)\left(1 + \lambda V_{DS}\right)\frac{\partial V_t}{\partial V_{BS}}$$

$$V_t = V_{t0} + \gamma\left(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right) \tag{1.140}$$

$$\frac{\partial V_t}{\partial V_{BS}} = -\frac{1}{2}\gamma\left(2\phi_f + V_{SB}\right)^{-1/2} = -\chi$$

χ = rate of change of threshold voltage with body bias voltage.

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = -k'\frac{W}{L}\left(V_{GS} - V_t\right)\left(1+\lambda V_{DS}\right)\frac{\partial V_t}{\partial V_{BS}}$$

$$g_{mb} = \frac{k'\frac{W}{L}\gamma\left(V_{GS} - V_t\right)\left(1+\lambda V_{DS}\right)}{\left[2\sqrt{\left(2\phi_f + V_{SB}\right)}\right]}$$

Since $g_m = k'\frac{W}{L}\left(V_{GS} - V_t\right)\left(1+\lambda V_{DS}\right)$, then

$\frac{g_{mb}}{g_m} = \frac{\gamma}{\left[2\sqrt{\left(2\phi_f + V_{SB}\right)}\right]} = \chi$ where

$$\gamma = \frac{1}{C_{ox}}\sqrt{2q\varepsilon N_A}$$

$$\phi_f = \frac{kT}{q}\ln\left[\frac{N_A}{n_i}\right]$$

$\chi = 0.1 \rightarrow 0.3$ (typical)

Hence, transconductance from the main gate (g_m) is typically 3 to 10 times larger than the transconductance from the body or the 2nd gate (g_{mb}).

If $\lambda V_{DS} << 1$, then

$$g_{mb} = \frac{k'\frac{W}{L}\gamma(V_{GS} - V_t)}{\left[2\sqrt{(2\phi_f + V_{SB})}\right]}$$

$$I_D = \frac{k'}{2}\frac{W}{L}(V_{GS} - V_t)^2 \text{ i.e } \sqrt{\frac{2L}{k'W}I_D} = (V_{GS} - V_t)$$

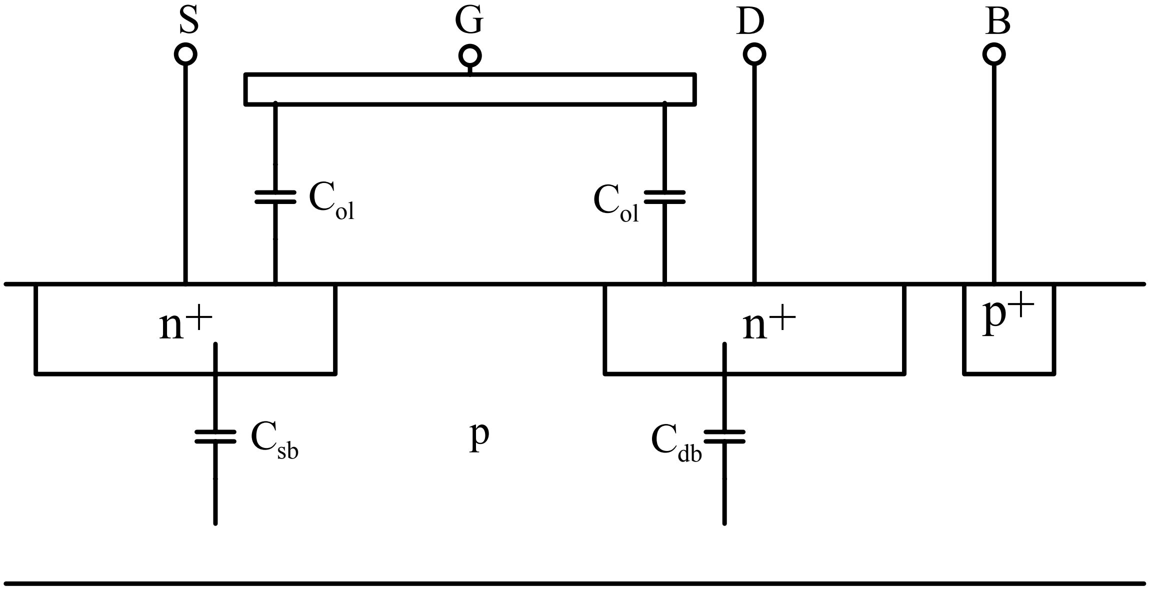
$$g_{mb} = \frac{k'\frac{W}{L}\gamma\sqrt{\frac{2L}{k'W}I_D}}{\left[2\sqrt{(2\phi_f + V_{SB})}\right]}$$

$$= \gamma\sqrt{\frac{k'(W/L)I_D}{2(2\phi_f + V_{SB})}}$$

1.6.7 Parasitic elements in the small-signal model

g_m, C_{gs}, C_{gd}, r_o and g_{mb} arise directly from essential processes in the device. Technological limitations in the fabrication introduce a number of parasitic elements that must be added to the equivalent circuit.

All p-n junctions should be rb during normal operation. Each junction exhibits a voltage-dependent parasitic capacitance associated with its depletion region.



$$C_{sb} = \frac{C_{sb0}}{\left(1+\frac{V_{SB}}{\Psi_0}\right)^{\frac{1}{2}}}$$

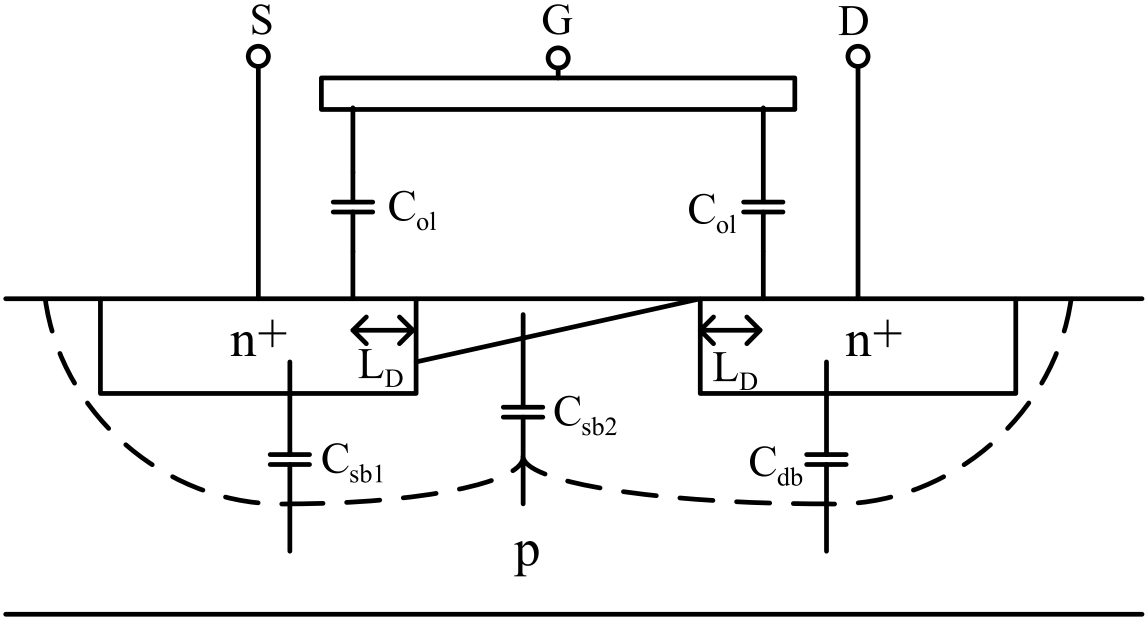
$$C_{db} = \frac{C_{db0}}{\left(1+\frac{V_{DB}}{\Psi_0}\right)^{\frac{1}{2}}}$$

Since the channel is attached to the S in the saturation or active region, C_{sb} also includes depletion-region capacitance from the induced channel to the body.

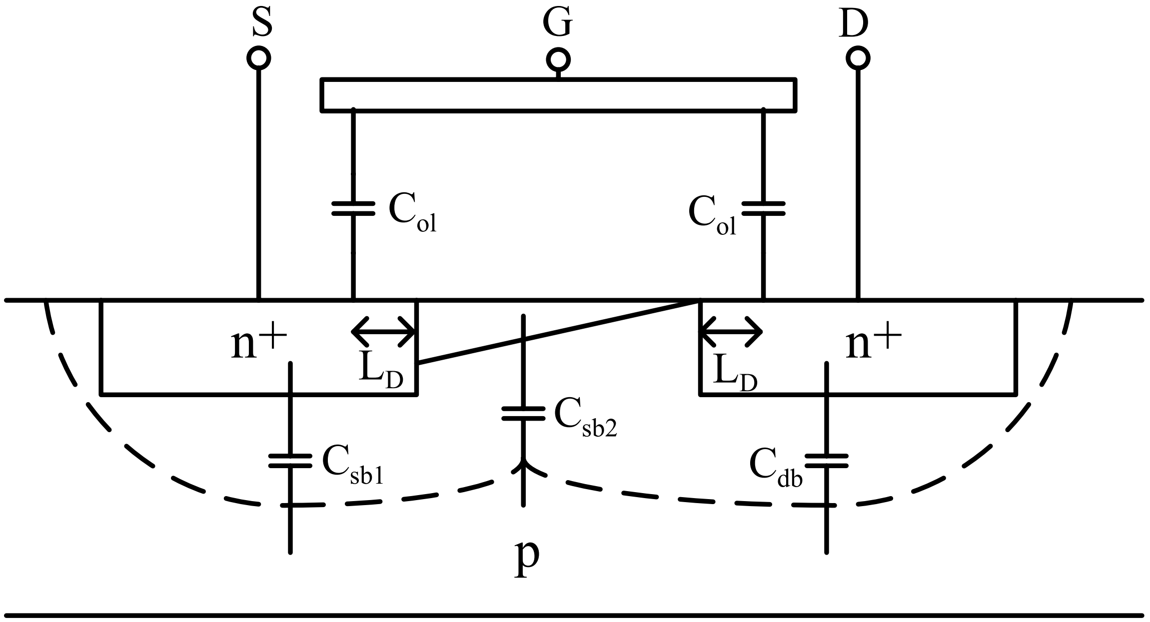
In triode region: $C_{gs} = C_{gd} = (1/2)C_{ox}WL$

In saturation/ active region: $C_{gs} = (2/3)C_{ox}WL$

$C_{gd} = 0$



In practice, the C_{gs} and C_{gd} values are increased due to the parasitic oxide capacitances arising from the gate overlap of the S and D regions. These capacitances are represented by C_{ol}.



1. <u>Cut-off operation:</u>

No channel, hence, $C_{gs} = C_{gd} = C_{ox}WL_d = C_{ol}$

2. <u>Triode/linear operation:</u>

$C_{gs} = C_{gd} = (1/2)C_{ox}WL + C_{ox}WL_d$

3. <u>Sat./active region:</u>

$C_{gs} = (2/3)C_{ox}WL + C_{ox}WL_d$

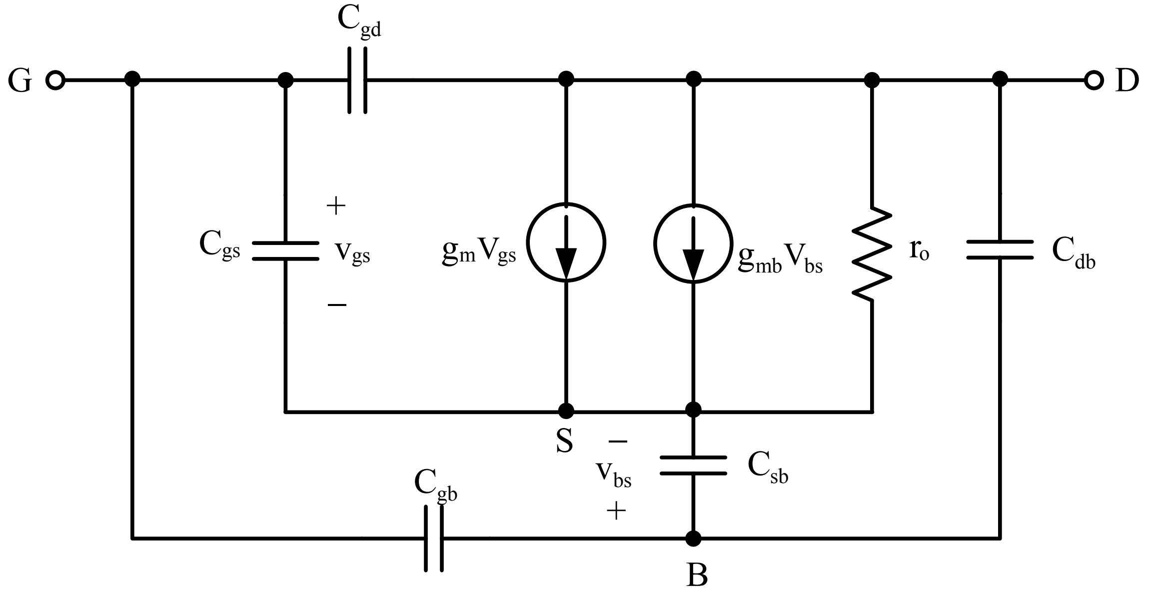
$C_{gd} = C_{ox}W\,L_d$

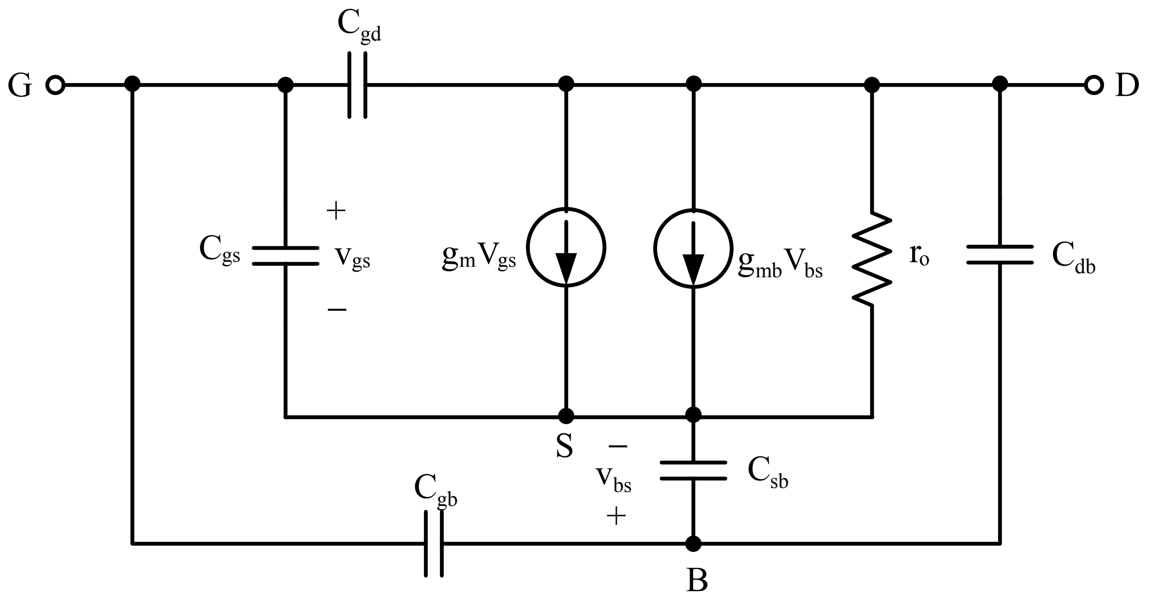
C_{gb} = parasitic oxide capacitance between G-channel material and the substrate outside the active-device area.

This capacitance is independent of the G-body voltage and models coupling from polysilicon and metal interconnects to the underlying substrate. This capacitor should be taken into account when simulating and calculating high-frequency circuit and device performance. Typical values depend on the oxide thickness. For SiO_2 thickness of $100\overset{o}{A}$, $C_{gb} = 3.45\ fF/\mu m^2$.

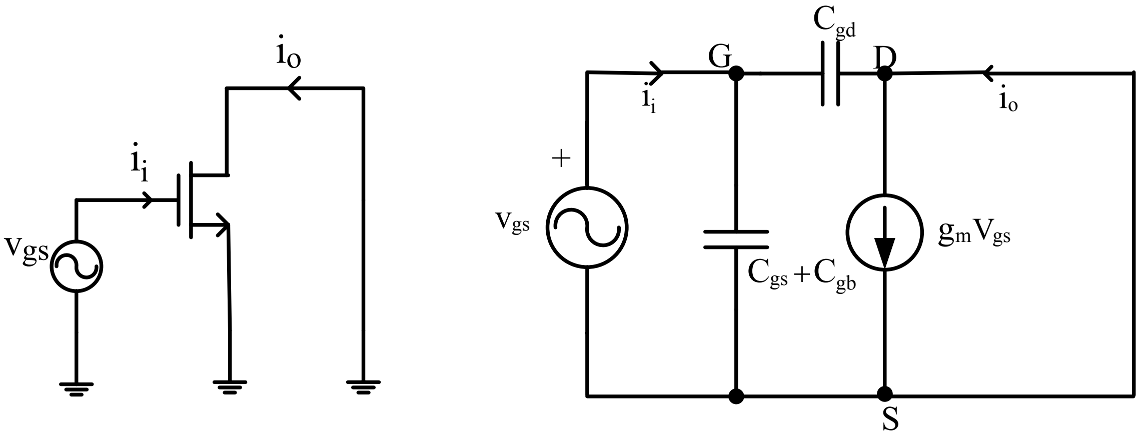
1.6.8 MOS transistor frequency response

Small-signal MOSFET equivalent circuit:





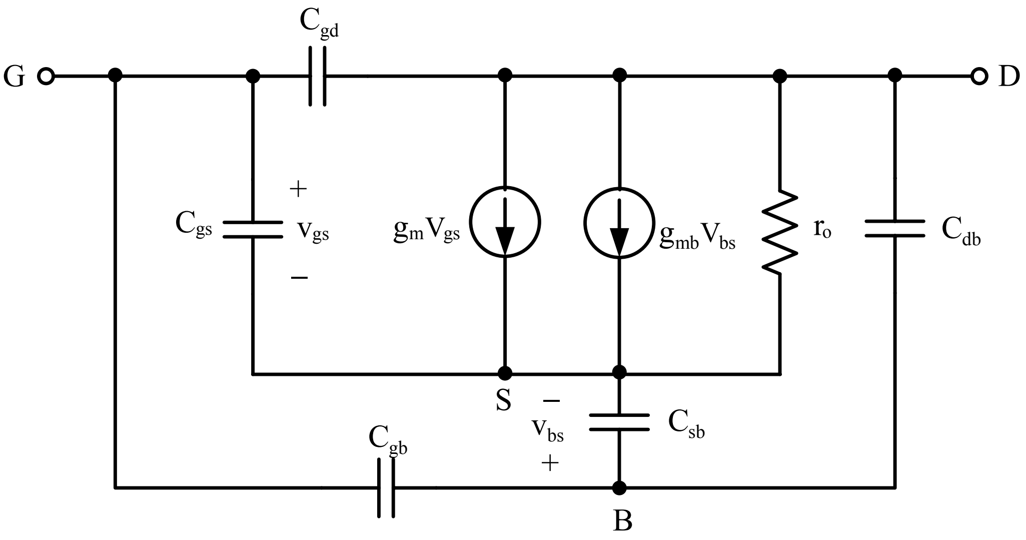
To determine f_T :



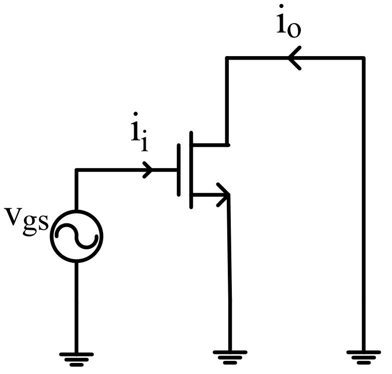
f_T = the frequency where the magnitude of the s/c, CS current gain falls to unity.

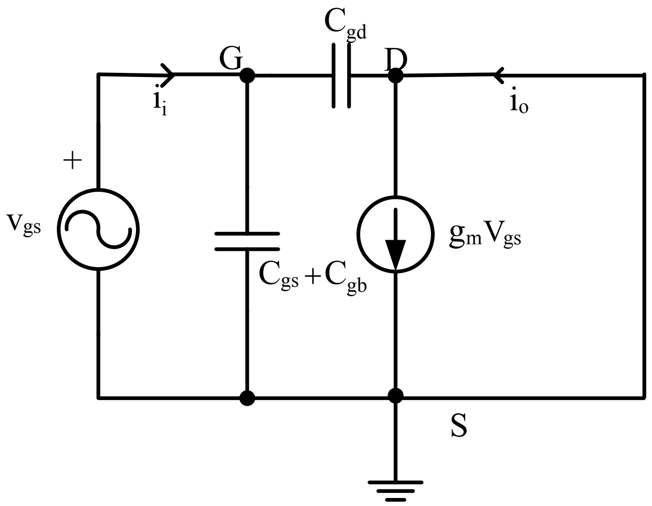
Although the dc $I_G = 0$, the high frequency behavior of the MOSFET is controlled by the capacitive elements in the small-signal model which cause I_G to increase as frequency increases.

Since $v_{sb} = v_{ds} = 0$, then $g_{mb}v_{bs}$ and r_o have no effect and are ignored as $g_{mb}v_{bs} = 0$ and r_o is s/c.



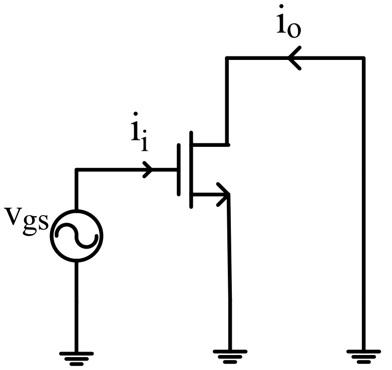
Since S, B and D are ac gnd, then C_{sb} and C_{db} have no effect on the calculations. C_{gs} is also in parallel with C_{gb} because of the same reason. Since D and S are both at ac gnd, then C_{gs} + C_{gb} is parallel to C_{gd}.

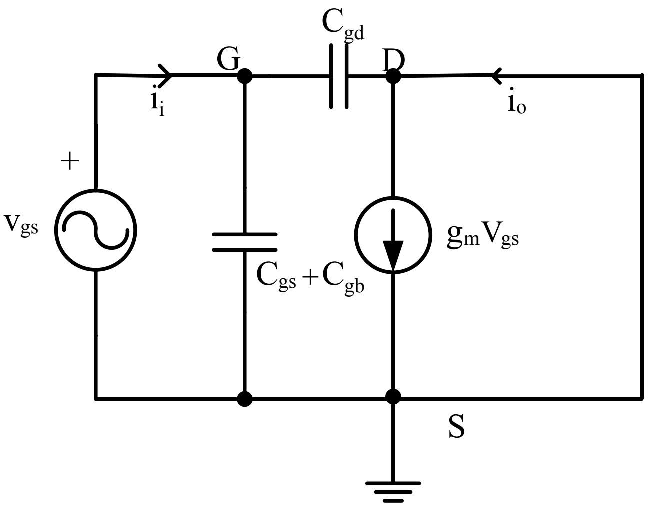




$$i_i = \frac{vgs}{\frac{1}{s\left[C_{gs}+C_{gb}+C_{gd}\right]}}$$

$$= s\left[C_{gs}+C_{gb}+C_{gd}\right]vgs$$





If the current fed forward through C_{gd} is neglected, then

$$i_o \approx g_m v_{gs}$$

$$i_i = s\left[C_{gs} + C_{gb} + C_{gd}\right] v_{gs}$$

$$\frac{i_o}{i_i} = \frac{g_m}{s\left[C_{gs} + C_{gb} + C_{gd}\right]}$$

$$\frac{i_o}{i_i}\left(j\omega\right) = \frac{g_m}{j\omega\left[C_{gs} + C_{gb} + C_{gd}\right]}$$

When the magnitude of the small-signal current gain = 1,

$$\left|\frac{i_o}{i_i}\right| = \frac{g_m}{\omega\left[C_{gs} + C_{gb} + C_{gd}\right]} = 1$$

$$\omega = \frac{g_m}{\left[C_{gs} + C_{gb} + C_{gd}\right]} = \omega_T$$

$$\omega=\frac{g_m}{\left[C_{gs}+C_{gb}+C_{gd}\right]}=\omega_T$$

$$f_T=\frac{g_m}{2\pi\left[C_{gs}+C_{gb}+C_{gd}\right]}$$

If $C_{gs} >> C_{gb} + C_{gd}$, then

$$f_T=\frac{g_m}{2\pi C_{gs}}$$

From $C_{gs}=\frac{2}{3}WLC_{ox}$ and $g_m=k'\frac{W}{L}\left(V_{GS}-V_t\right)$,

$$f_T=\frac{\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_t)}{2\pi\left(\frac{2}{3}\right)WLC_{ox}}$$

$$=\frac{1.5\mu_n\left(V_{GS}-V_t\right)}{2\pi L^2}$$

In order to increase f_T , V_{OV} has to be in the order of hundreds mV. With the advancement in integrated circuit technology (where transistor becomes smaller and therefore L↓), f_T ↑.

$\tau_T = 1 / \omega_T$

For a BJT,

$\tau_T = \tau_F + \frac{C_{je}}{g_m} + \frac{C_\mu}{g_m}$ where

τ_F = B transit time in the forward direction.

C_μ = B-C parasitic capacitance

C_{je} = B-E parasitic capacitance

When the parasitic depletion-layer capacitance is neglected, the BJT has $\tau_F \gg \frac{C_{je}}{g_m} + \frac{C_\mu}{g_m}$. Hence,

$\tau_T \approx \tau_F$

$f_T = \frac{1}{2\pi\tau_F}$

From $\tau_F = \frac{W_B^2}{2D_n}$ (1.99)

$f_T = \frac{2D_n}{2\pi W_B^2}$

From Einstein relationship, $V_T = \frac{D_n}{\mu_n}$

$f_{T\_BJT} = 2\frac{\mu_n V_T}{2\pi W_B^2}$

$$f_{T\_BJT} = 2\frac{\mu_n V_T}{2\pi {W_B}^2}$$

$$f_{T\_MOS} = \frac{1.5\mu_n(V_{GS} - V_t)}{2\pi L^2}$$

In both the equations above,

1. f_T increases as the inverse square of the critical device dimension across which carriers are in transit decreases.
2. V_T = 26 mV is fixed for BJT but f_T of a MOSFET can be increased by operating at high values of V_{OV}.
3. W_B (the B width) is a vertical dimension determined by diffusions or implants and typically be made much smaller than L of MOSFET which depends on surface geometry and photolithographic processes. BJT generally has higher f_T than MOSFET made with comparable processing.