

# EEE130 Digital Electronics I

## Lecture #3

- Logic Gates -

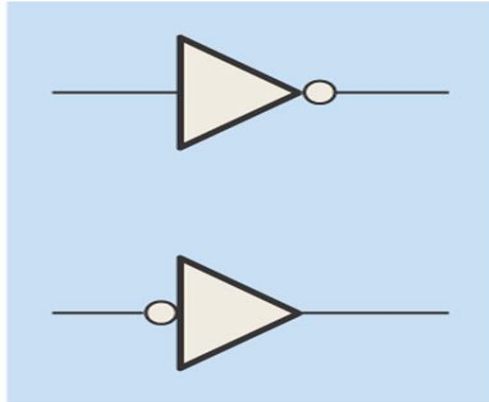
By Dr. Shahrel A. Suandi

# Topics to be discussed

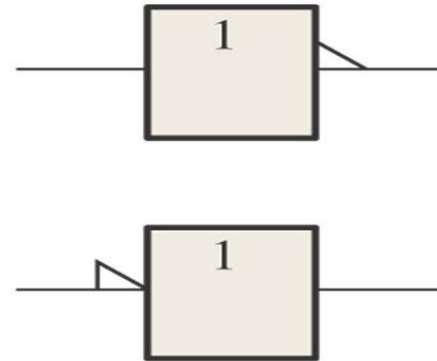
- 3-1 The Inverter
- 3-2 The AND Gate
- 3-3 The OR Gate
- 3-4 The NAND Gate
- 3-5 The NOR Gate
- 3-6 The Exclusive-OR and Exclusive-NOR Gates

- 3-7 Programmable Logic
- 3-8 Fixed-Function Logic
- 3-9 Troubleshooting

# 3-1 The Inverter



(a) Distinctive shape symbols with negation indicators

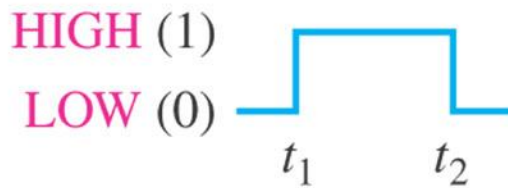
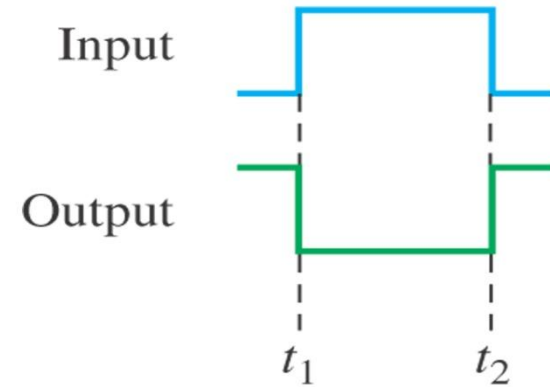


(b) Rectangular outline symbols with polarity indicators

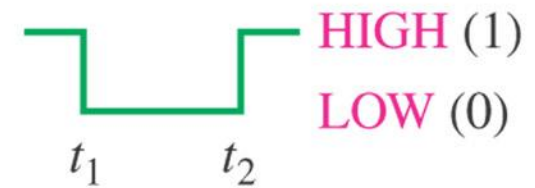
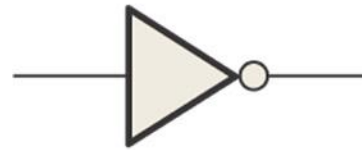
- Be careful of the bubble (“ ° ”) usage – to show active-LOW
- The triangle symbol in (b) indicates inversion

# Inverter Truth Table

INPUT	OUTPUT
0	1
1	0

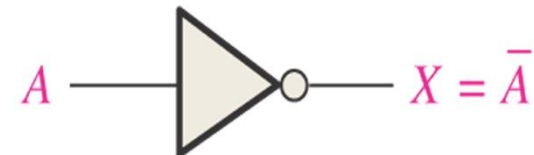


Input pulse



Output pulse

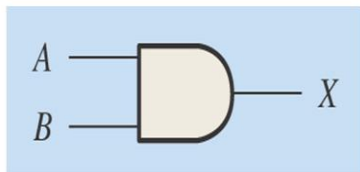
Logic expression:  $X = \bar{A}$



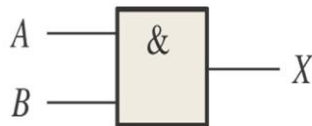
# 3-2 The AND Gate

- Significant about AND gate:
  - It produces a HIGH output only when *all of the inputs are HIGH*
- The truth table:

Inputs		Outputs
0	0	0
0	1	0
1	0	0
1	1	1



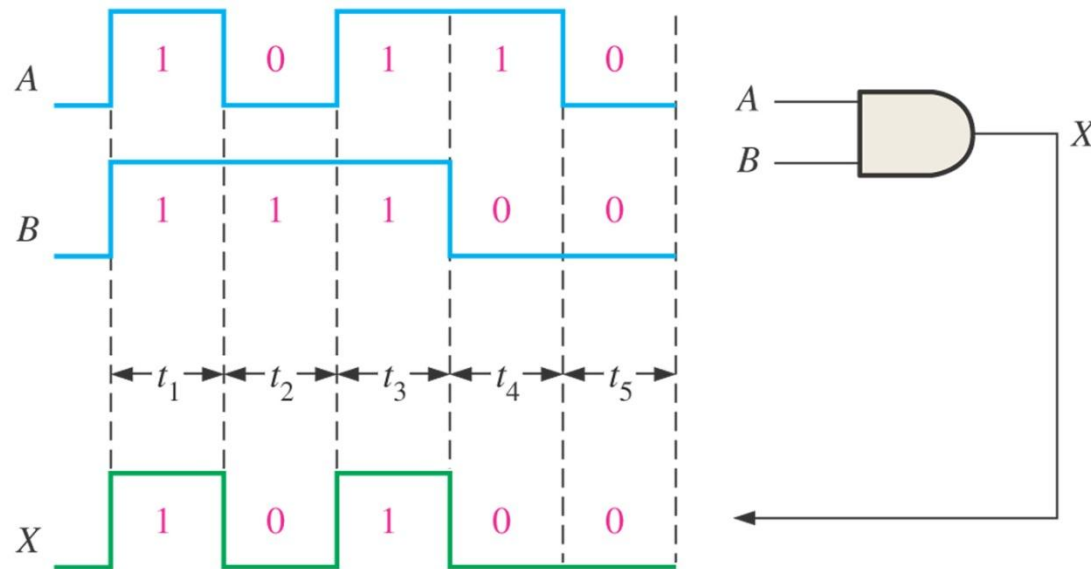
(a) Distinctive shape



(b) Rectangular outline with the AND (&) qualifying symbol

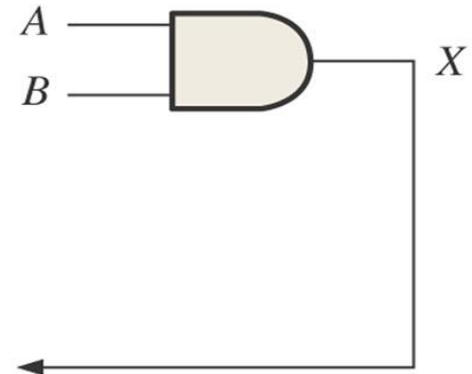
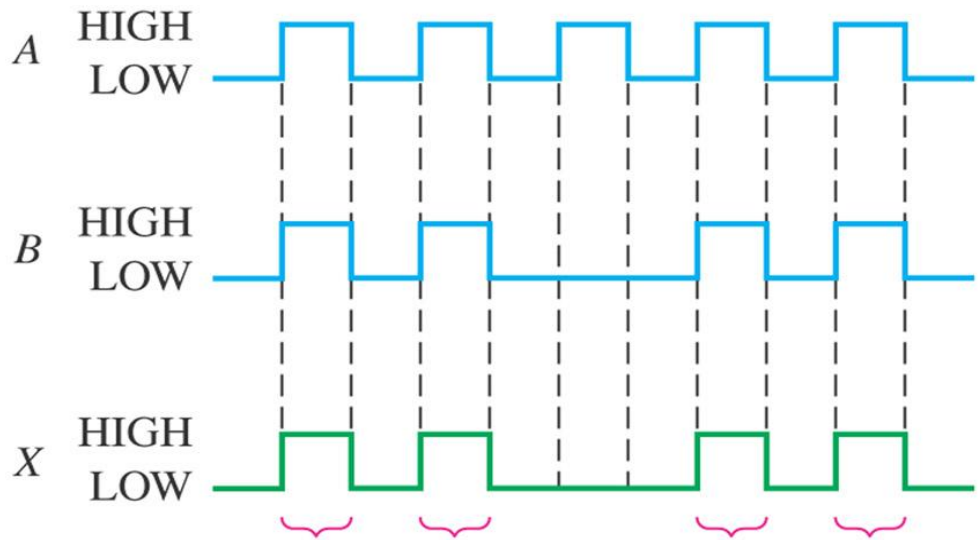
# More about AND gate

- Combination can be made from AND gate
  - Depending on the input variables  $N = 2^n$  where  $n$  is the total of inputs
- Operation with waveform inputs



# Example 3-3

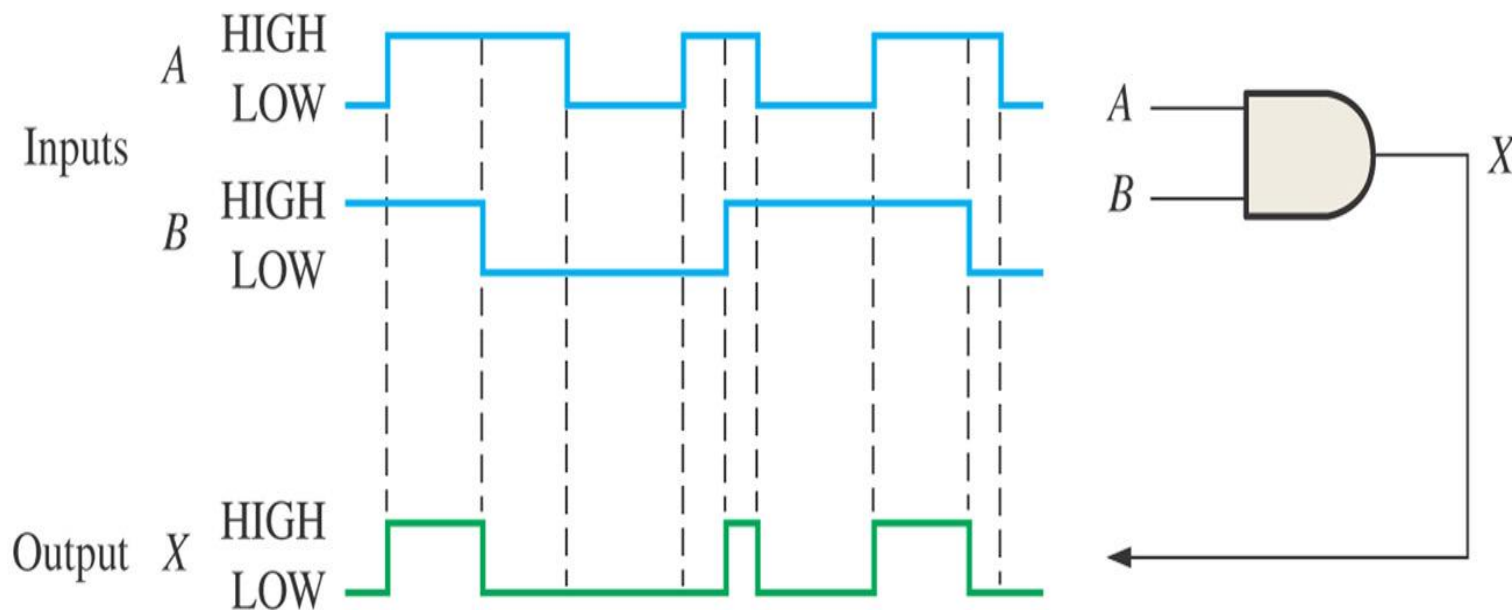
- If two waveforms, A and B, are applied to the AND gate inputs, what is the resulting output waveform?



*A and B are both HIGH during these four time intervals.  
Therefore X is HIGH.*

# Example 3-4

- For the two input waveforms, A and B, show the output waveform with its proper relation to the inputs.





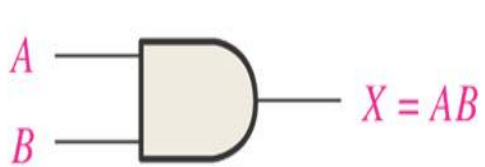
# Logic expression for AND gate

- The logical AND function of two variables is represented mathematically either by placing a dot between the two variable, or by writing the adjacent letter without the dot

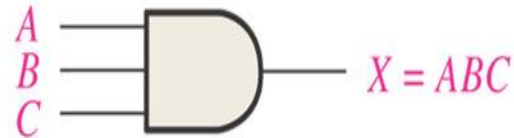
–  $A \cdot B$  or  $AB$

- Boolean multiplication = AND function

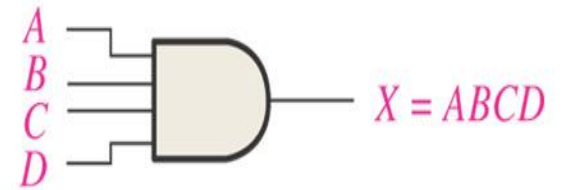
# Advance for AND gate



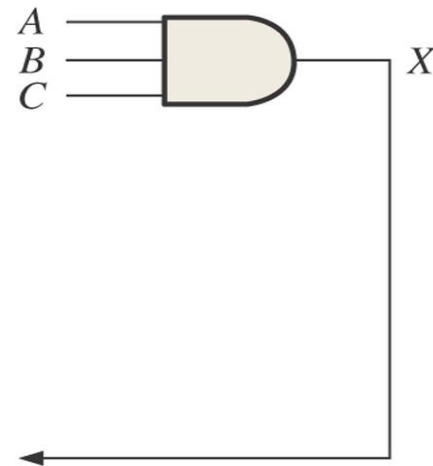
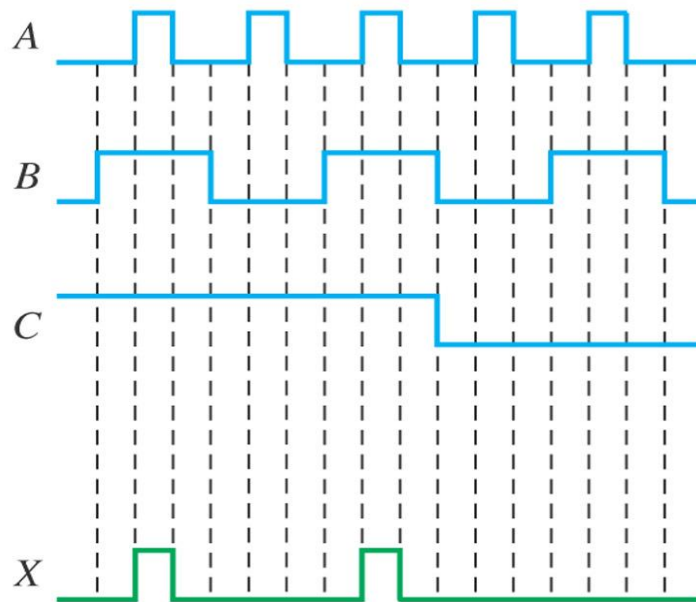
(a)



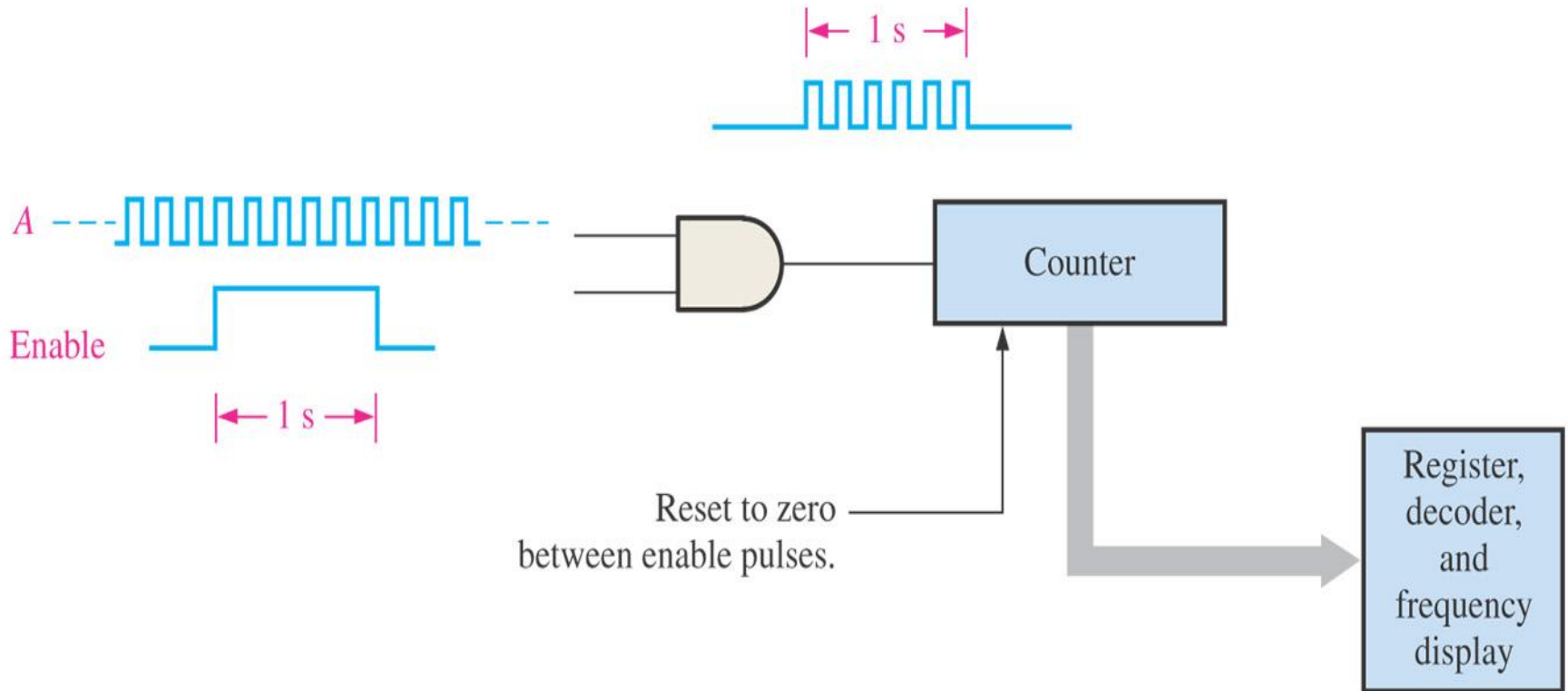
(b)



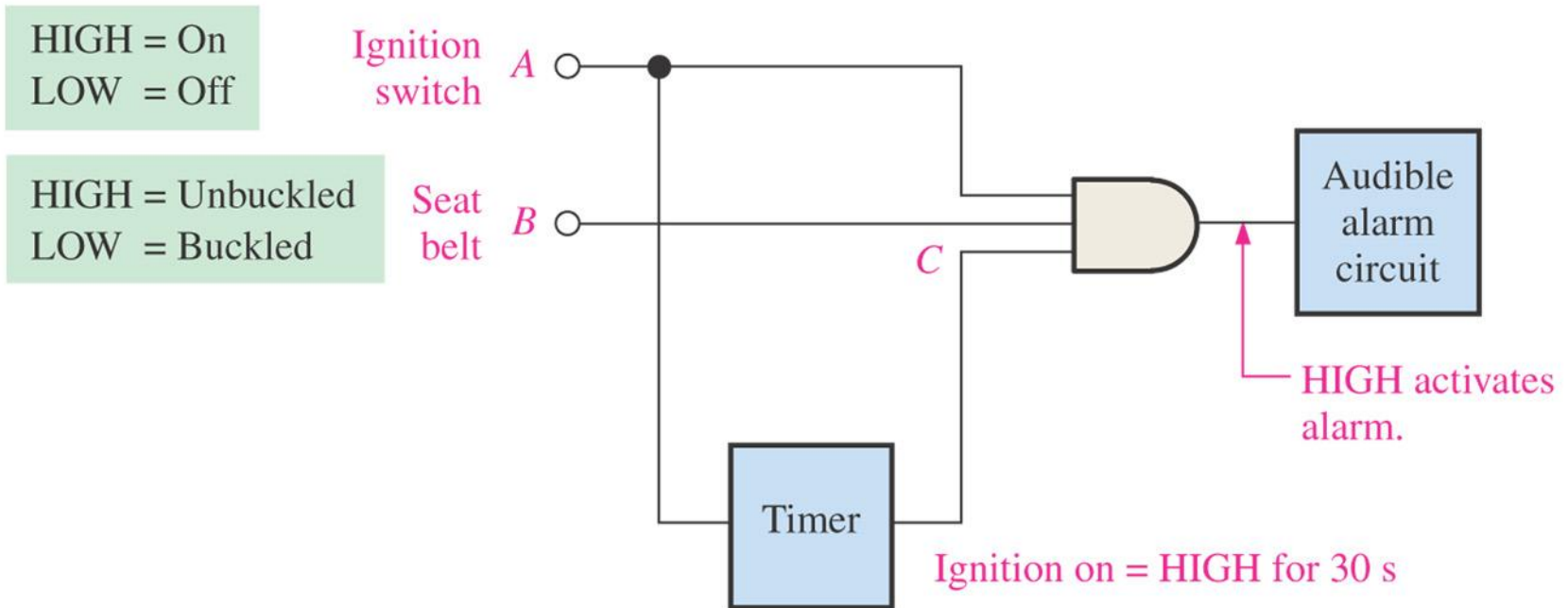
(c)



# Applications – the AND gate as an enable/inhibit device



# Applications – A seat belt alarm system

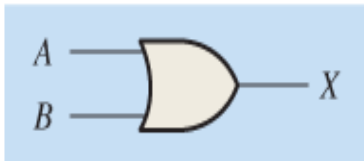


# 3-3 The OR Gate

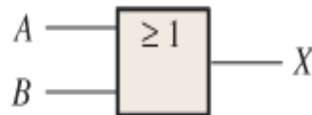
- Significant about OR gate:
  - It produces a HIGH on the output when any of the inputs is HIGH

- The truth table:

Inputs		Outputs
0	0	0
0	1	1
1	0	1
1	1	1



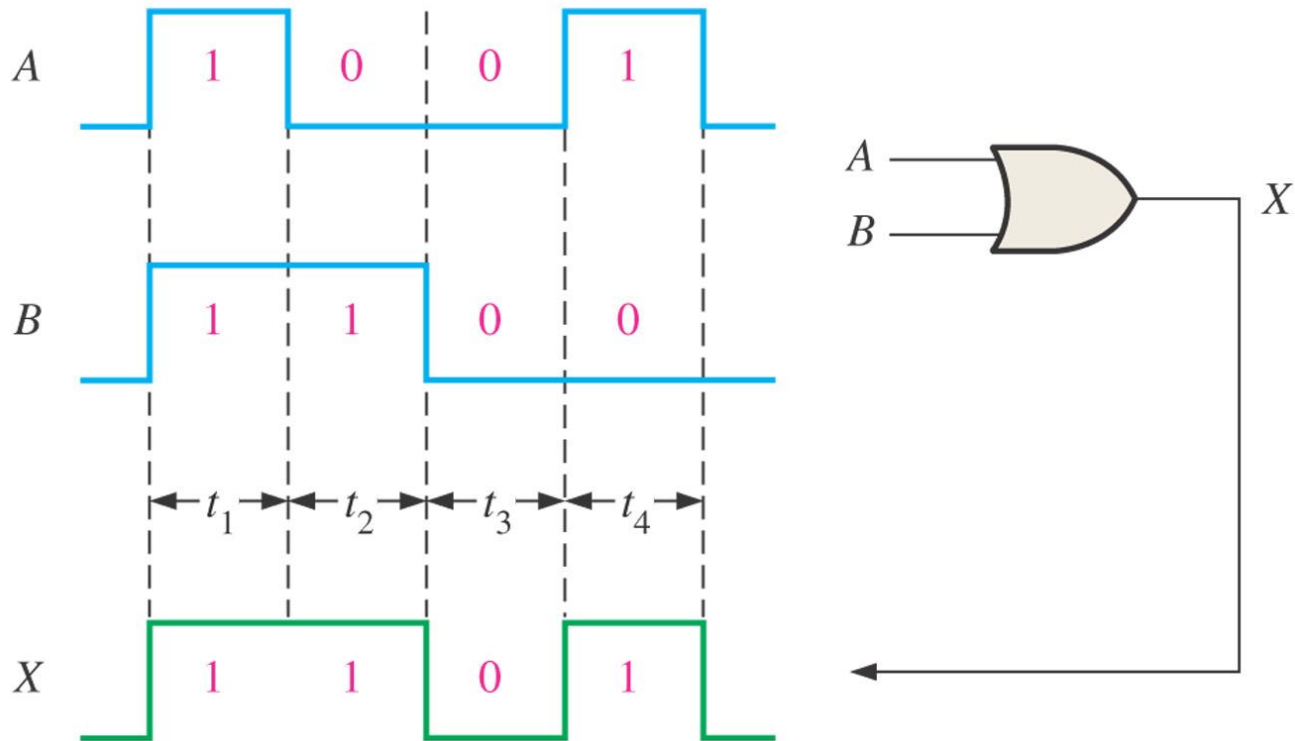
(a) Distinctive shape



(b) Rectangular outline with the OR ( $\geq 1$ ) qualifying symbol

# More about OR gate(1)

- Operation with waveform inputs



# More about OR gate(2)

- Logic expression for an OR gate

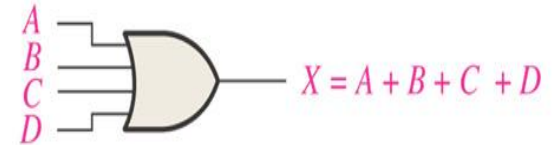
$$X = A + B$$



(a)



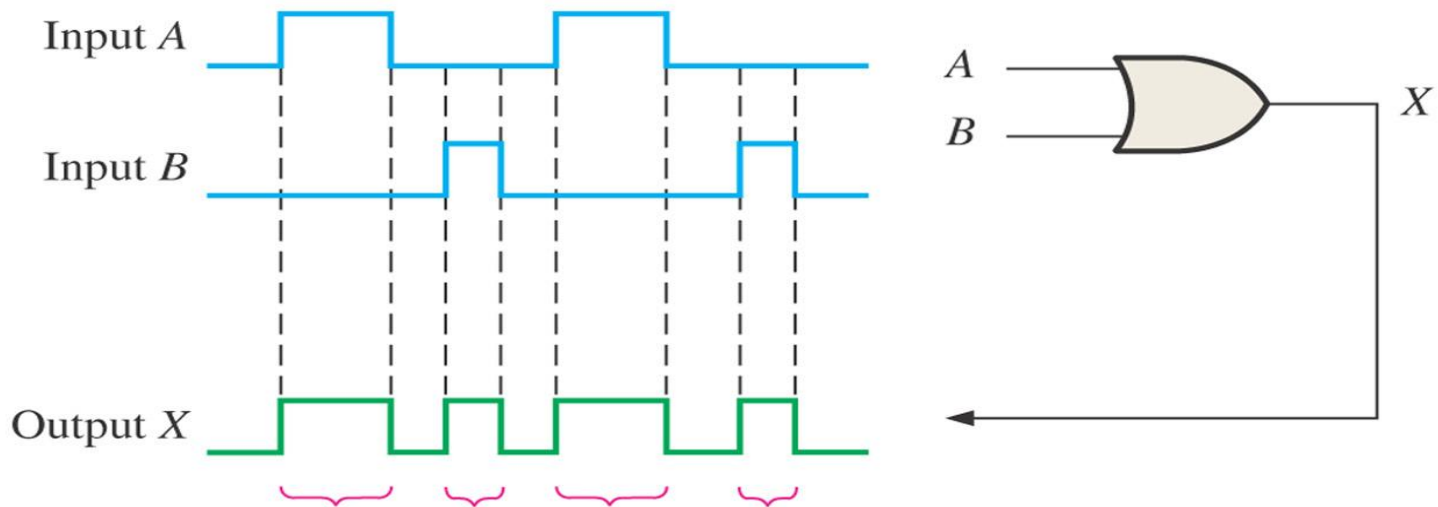
(b)



(c)

# Example 3-6

- If the two input waveforms, A and B, are applied to the OR gate, what is the resulting output waveform?

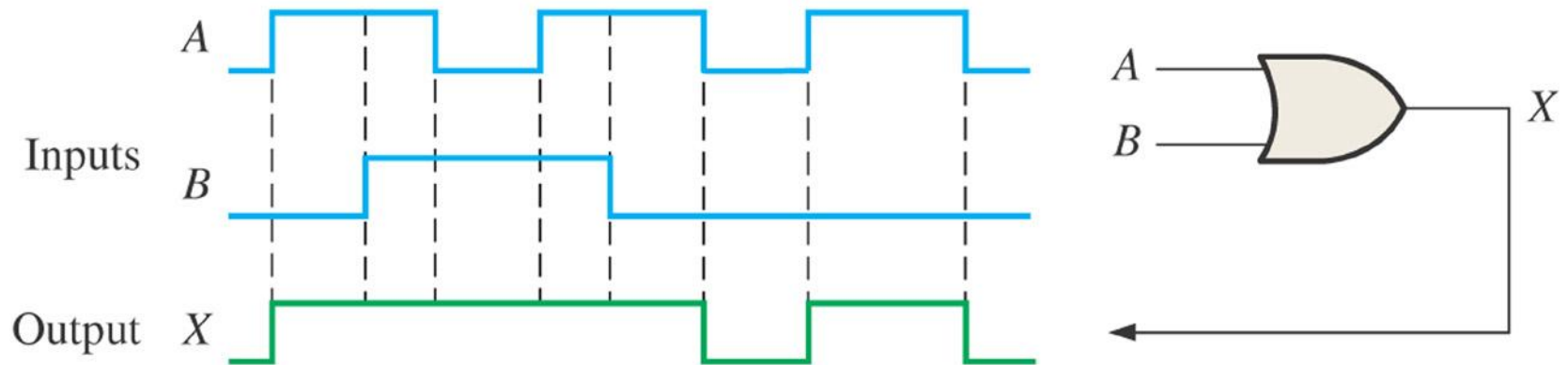


When either input or both inputs are HIGH, the output is HIGH.



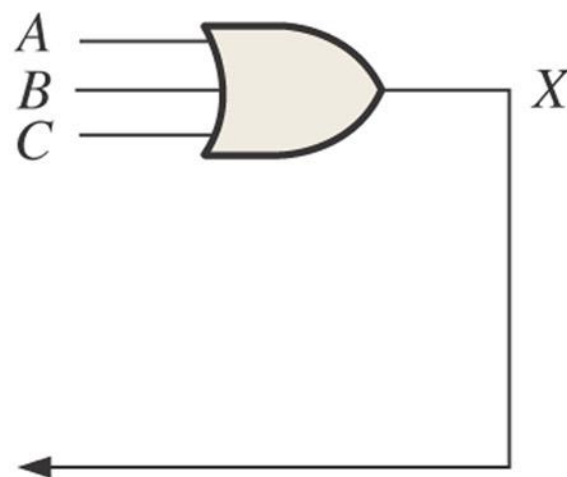
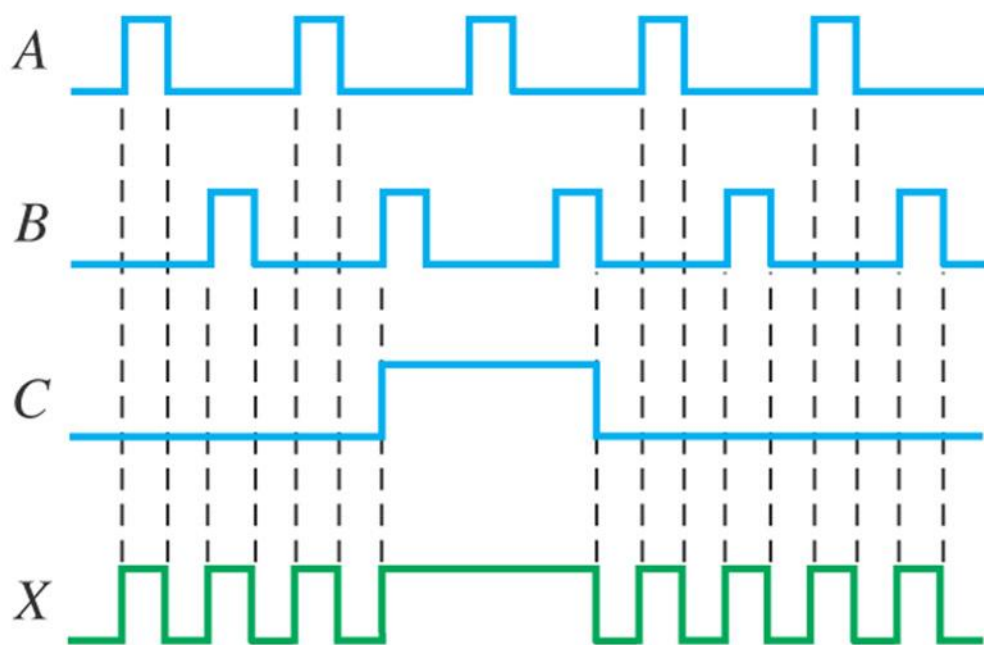
# Example 3-7

- For the two input waveforms, A and B, show the output waveform with its proper relation to the inputs



# Example 3-8

- For the 3-input OR gate, determine the output waveform in proper time relation to the inputs

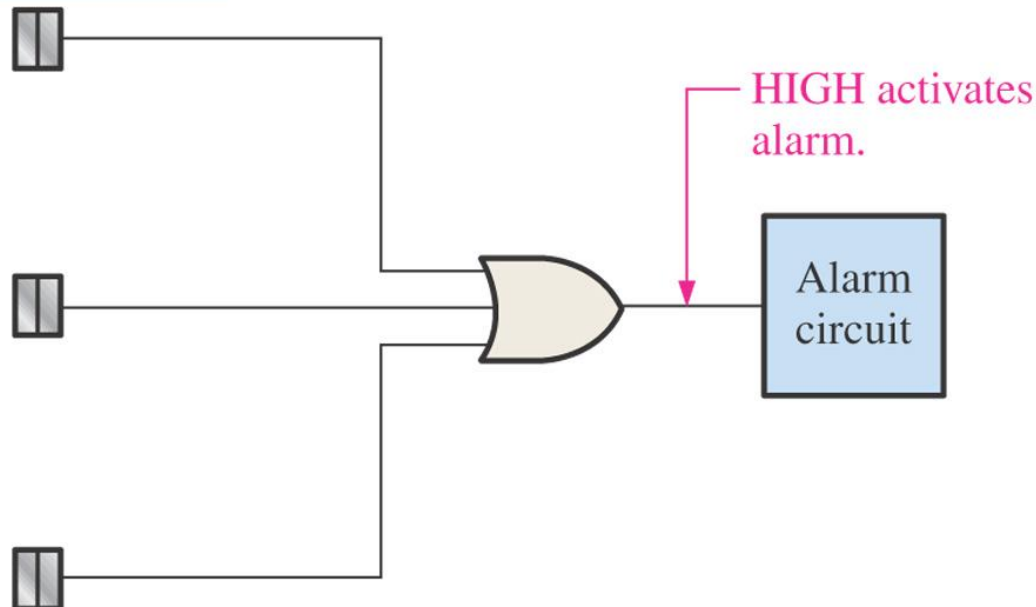


# An application

- Intrusion detection and alarm system

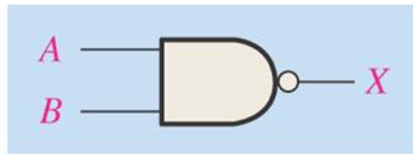
Open door/window  
sensors

HIGH = Open  
LOW = Closed

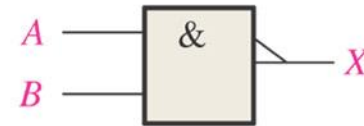
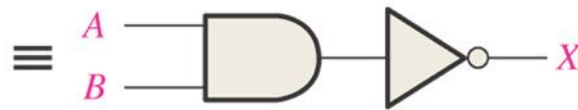


# 3-4 The NAND Gate

- It produces a LOW output only when all the inputs are HIGH



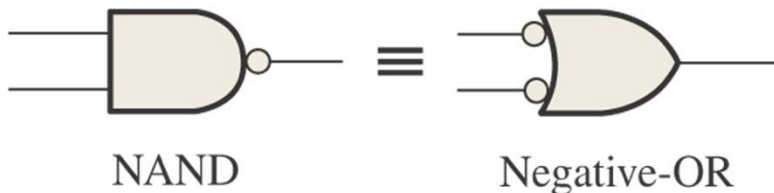
(a) Distinctive shape, 2-input NAND gate and its NOT/AND equivalent



(b) Rectangular outline, 2-input NAND gate with polarity indicator

Logic expression:

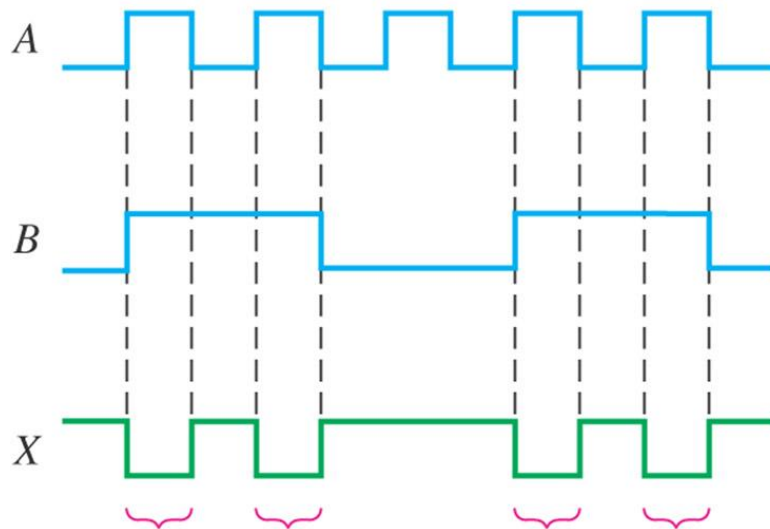
$$X = \overline{AB}$$



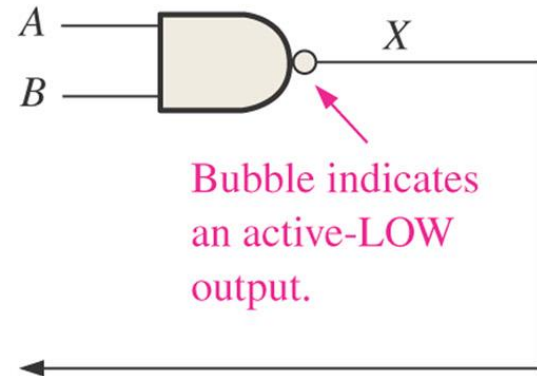
Inputs		Outputs
0	0	1
0	1	1
1	0	1
1	1	0

# Example 3-9

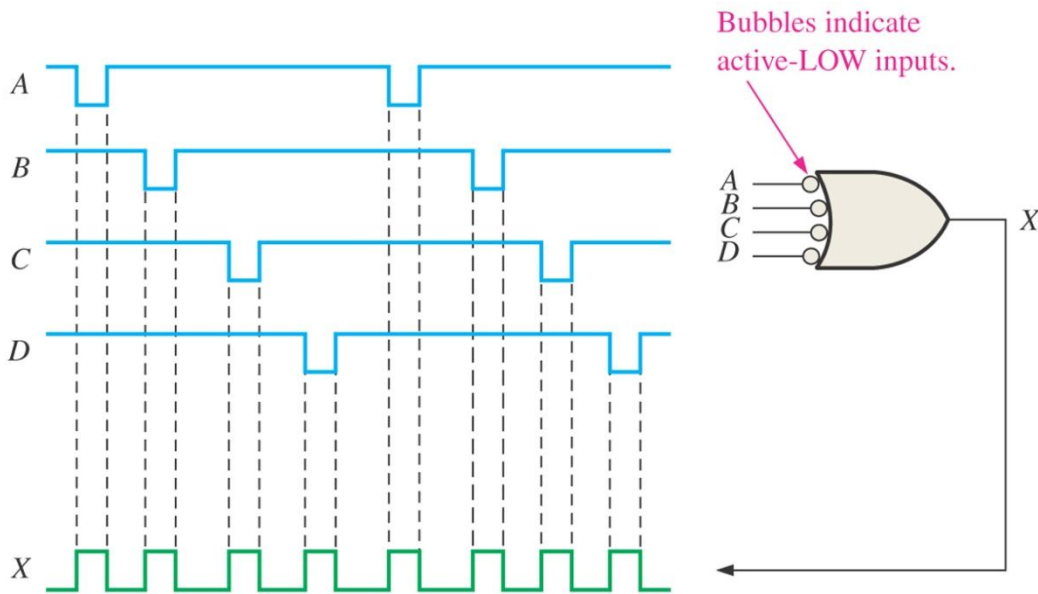
- If the two waveforms, A and B, are applied to the NAND gate inputs, determine the resulting output waveform



A and B are both HIGH during these four time intervals. Therefore X is LOW.



# Example 3-13 – 4-input NAND operating as negative-OR



NAND

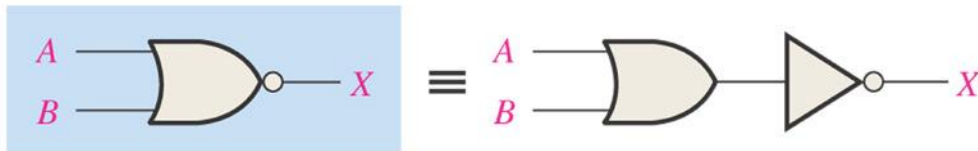
Input				Out put
A	B	C	D	X
1	1	1	1	0
0	1	1	1	1
1	1	1	1	0
1	0	1	1	1

Neg-OR

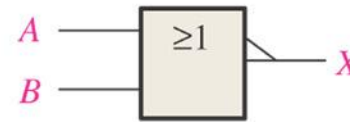
Input				Out put
A	B	C	D	X
1	1	1	1	0
0	1	1	1	1
1	1	1	1	0
1	0	1	1	1

# 3-5 The NOR Gate

- It produces a LOW output when any of its inputs is HIGH



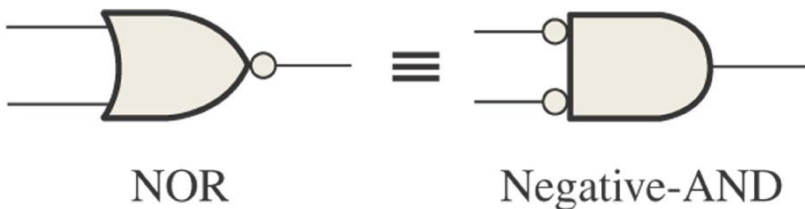
(a) Distinctive shape, 2-input NOR gate and its NOT/OR equivalent



(b) Rectangular outline, 2-input NOR gate with polarity indicator

Logic expression:

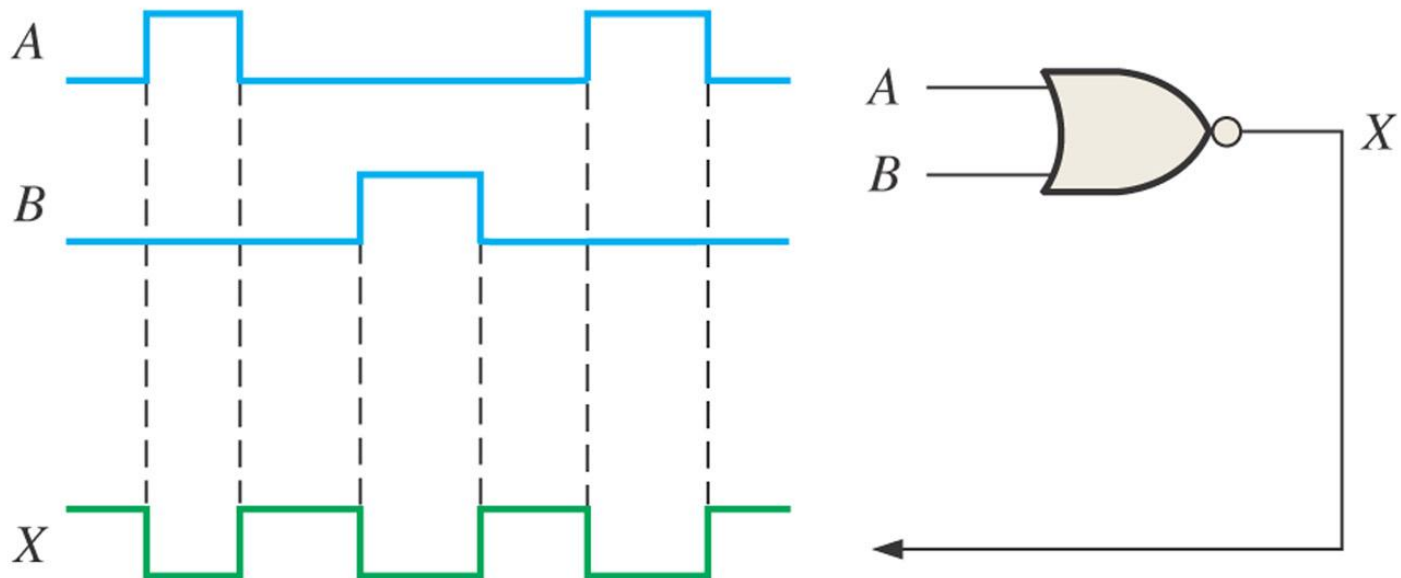
$$X = \overline{A + B}$$



Inputs		Outputs
0	0	1
0	1	0
1	0	0
1	1	0

# Example 3-14

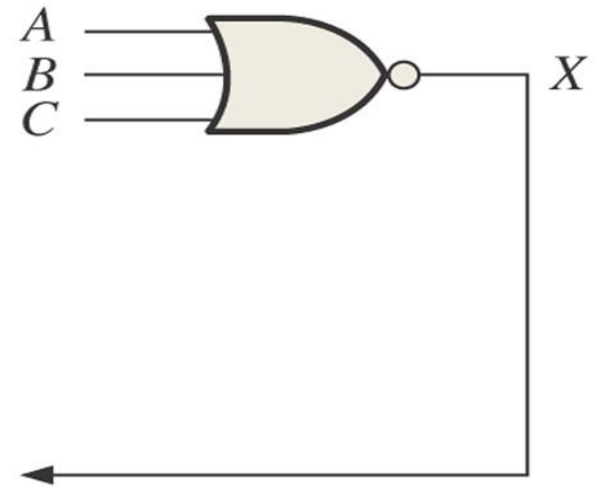
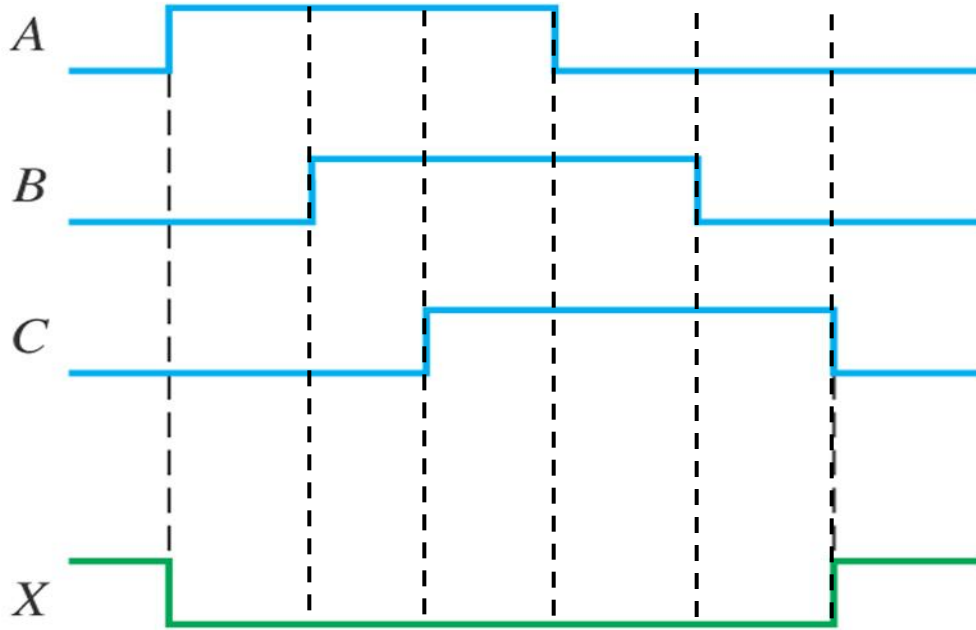
- If the two waveforms, A and B, are applied to a NOR gate, what is the resulting output waveform?



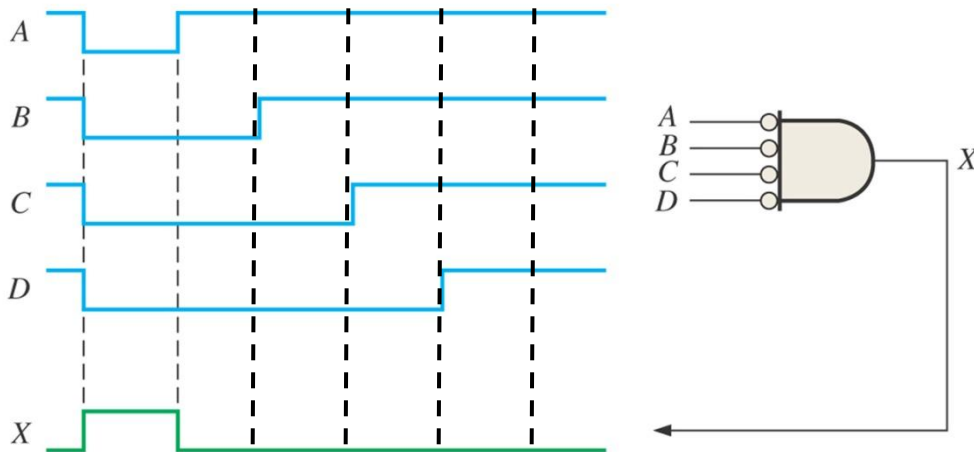


# Example 3-15

- Show the output waveform for the 3-input NOR gate with the proper time relation to the inputs.



# Example 3-18 – 4-input NOR gate operating on negative-AND gate



NOR

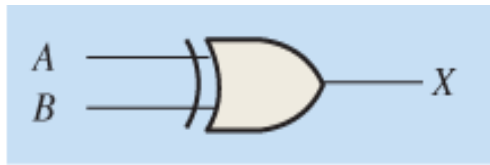
Input				Out put
A	B	C	D	X
1	1	1	1	0
0	0	0	0	1
1	0	0	0	0
1	1	0	0	0

Neg-AND

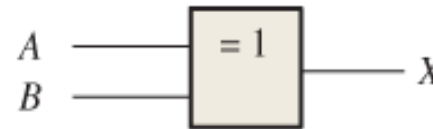
Input				Out put
A	B	C	D	X
1	1	1	1	0
0	0	0	0	1
1	0	0	0	0
1	1	0	0	0

# 3-6(1) The Exclusive-OR

- The output is HIGH only when the two inputs are at opposite logic levels (has only two inputs)
- Exclusive OR is written as **XOR** and the symbols are given below



(a) Distinctive shape

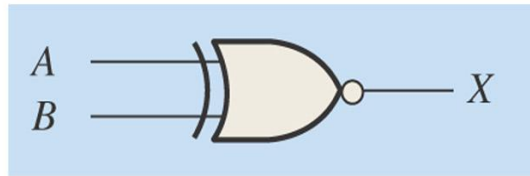


(b) Rectangular outline with the XOR

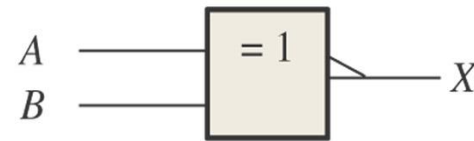
Inputs		Outputs
0	0	0
0	1	1
1	0	1
1	1	0

# 3-6(2) The Exclusive-NOR Gates

- The output is LOW only when the two inputs are at opposite logic levels (has only two inputs)
- The exclusive-NOR gate is written as **XNOR** and the symbol is written below



(a) Distinctive shape

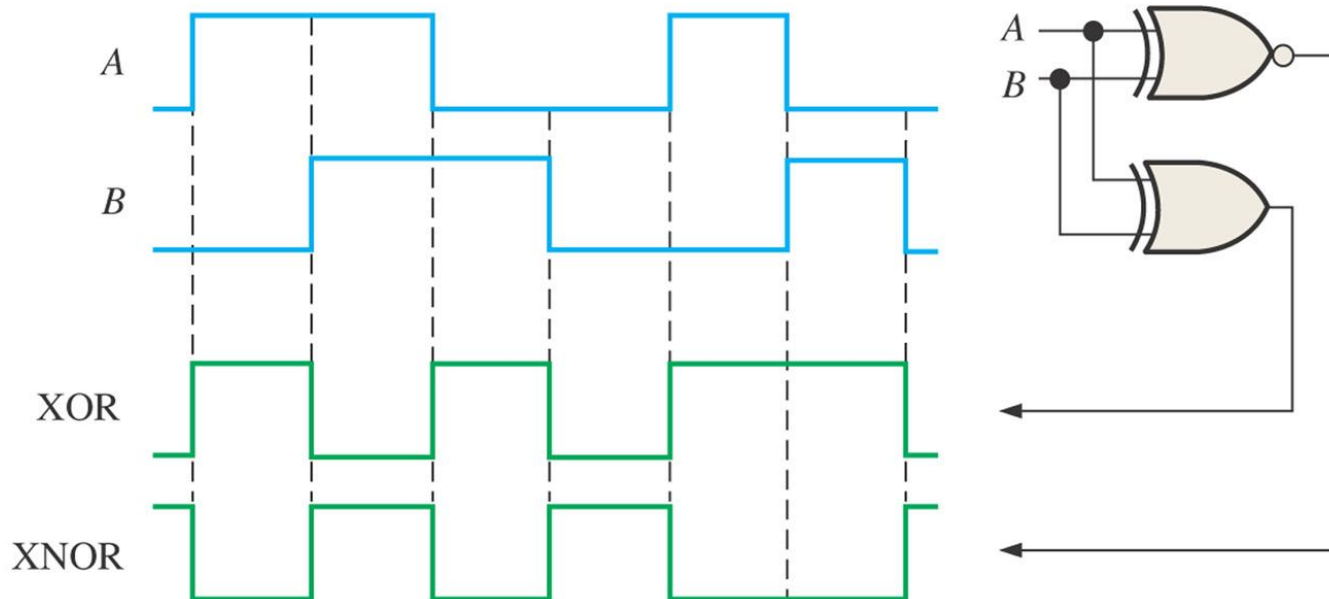


(b) Rectangular outline

Inputs		Outputs
0	0	1
0	1	0
1	0	0
1	1	1

# Example 3-20

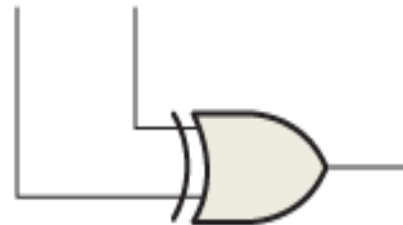
- Determine the output waveforms for the XOR gate and for the XNOR gate, given the following inputs.



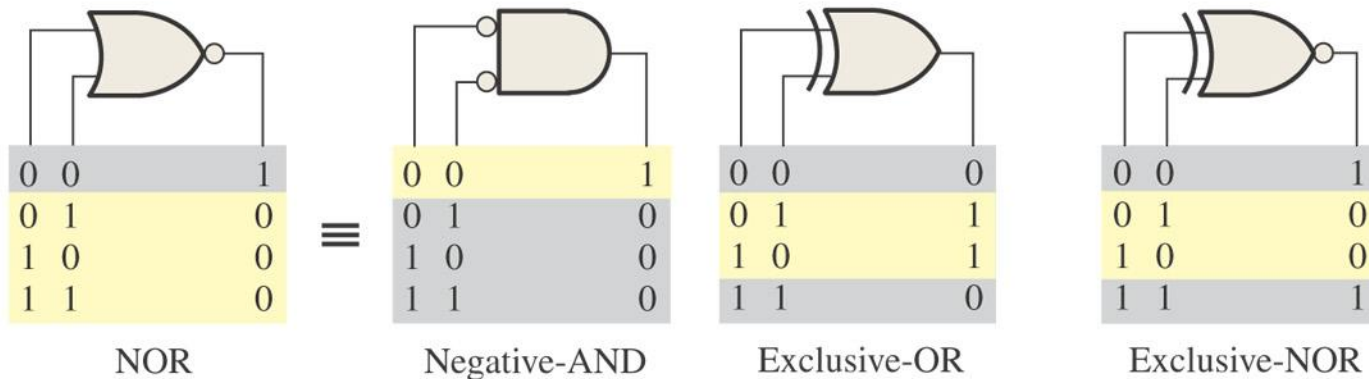
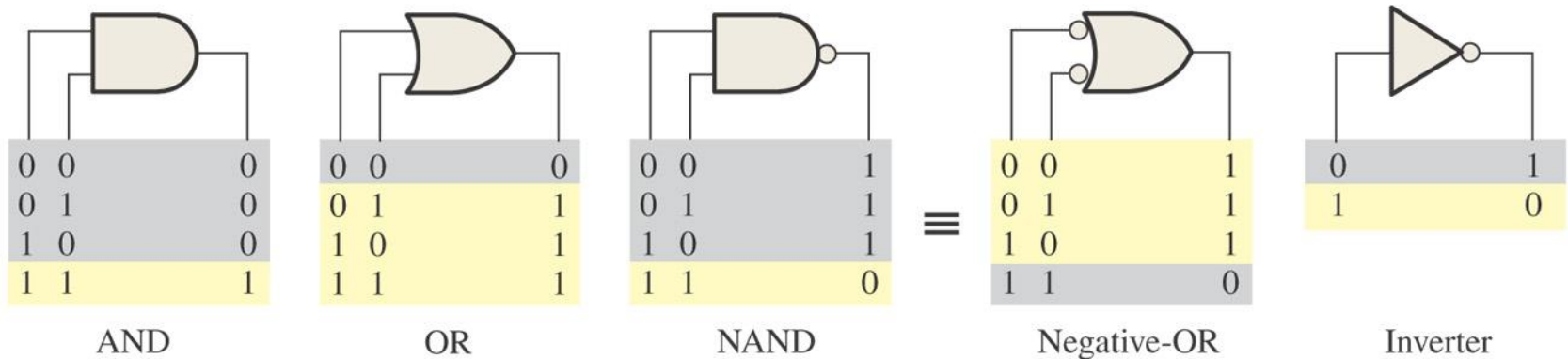
# Application of XOR – as a two-bit adder

- From Chapter 2, we know that the basic rules for binary addition are:  $0+0=0$ ,  $0+1=1$ ,  $0+1=1$  and  $1+1=10$ . In the last rule, if we need to discard the second bit (1), we can use XOR
- Why??
  - Please refer to the truth table on the right

Input bits		Output (sum)
A	B	$\Sigma$
0	0	0
0	1	1
1	0	1
1	1	0 (without 1 carry)



# Summary of Logic Gates



Note: Active states are shown in yellow.