EEE130 Digital Electronics I
Lecture #6

- Functions of Combinational Logic -

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Topics to be covered

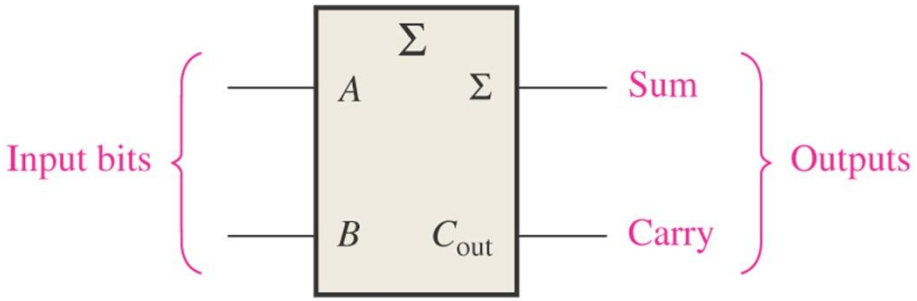
- 6-1 Basic Adders
- 6-2 Parallel Binary Adders
- 6-3 Ripple Carry versus Look-Ahead Carry Adders
- 6-4 Comparators
- 6-5 Decoders
- 6-6 Encoders
- 6-7 Code Converters
- 6-8 Multiplexers (Data Selectors)
- 6-9 Demultiplexers
- 6-10 Parity Generator/Checkers

6-1 Basic Adders

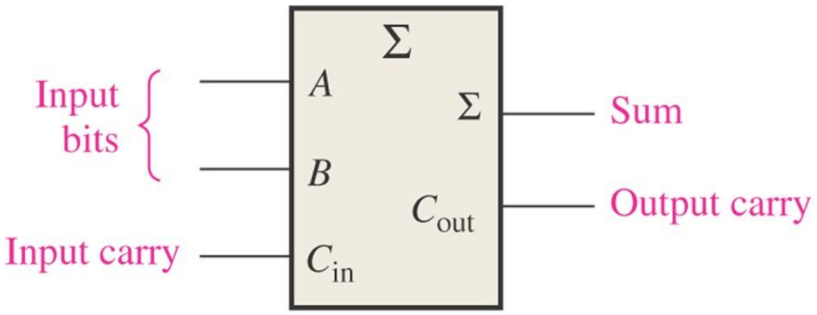
- There are full-adder and half-adder
- Half-adder:
  - The half-adder accepts two binary digits on its inputs and produces two binary digits on its outputs, a sum bit and a carry bit
  - Similar to XOR
- Full-adder:
  - The full-adder accepts two input bits and an input carry and generates a sum output and an output carry

Symbols used for adders

Half-adder



Full-adder



A	B	Cout	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

A	B	Cin	Cout	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

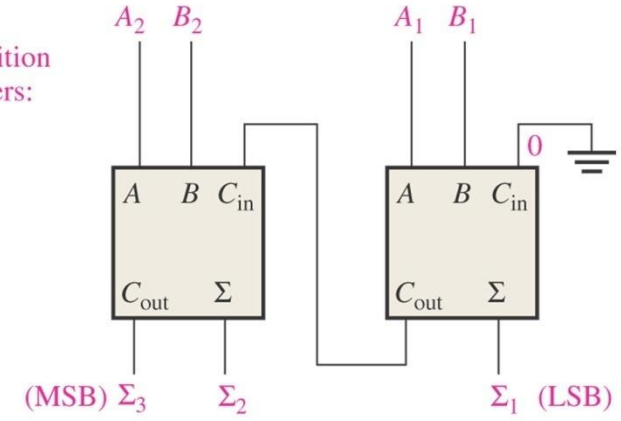
6-2 Parallel Binary Adders

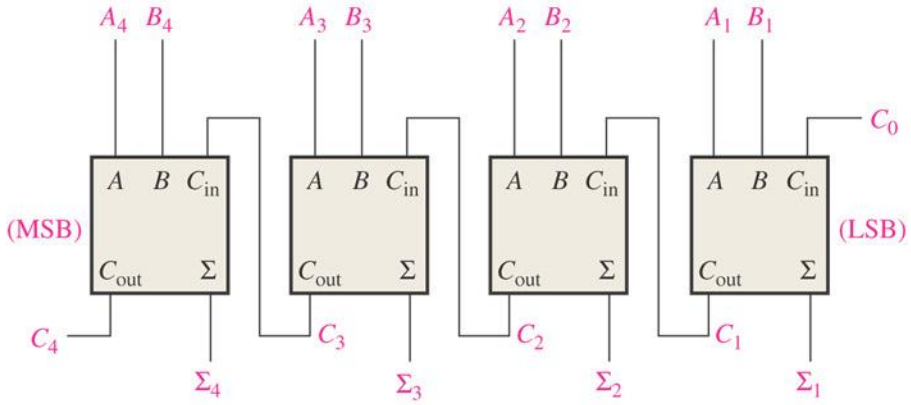
- More than two full-adders can be connected to form parallel binary adders
- How they are arranged?
  - Parallel/cascade by connecting C_{out} from the lower bit to C_{in} in a higher bit
- Why they are needed?
  - To add binary numbers more than 2 bits; ie. For 2-bit numbers, 2 adders are needed; 4-bit numbers, 4 adders are needed, and so on
- What important things that we should remember?
  - A full adder can be used instead of half adder – the LSB concerned full adder must be connected to ground
  - Let's see everything graphically…

Block diagram of 2-bit and 4-bit parallel adders

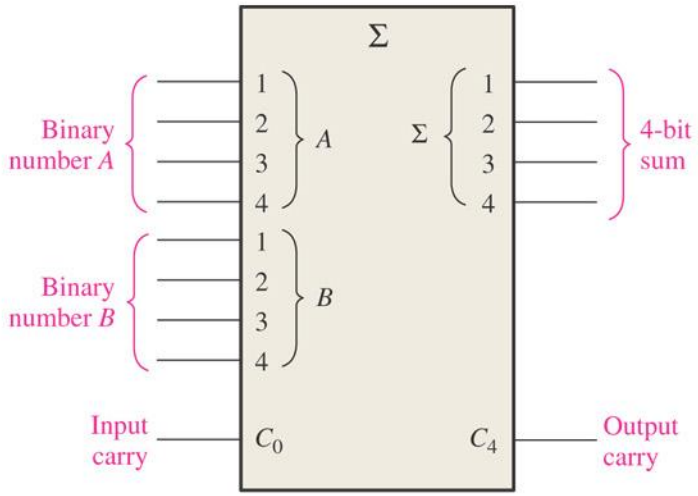
General format, addition of two 2-bit numbers:

$$\begin{array}{r} A_2A_1 \\ +\ B_2B_1 \\ \hline \Sigma_3\Sigma_2\Sigma_1 \end{array}$$



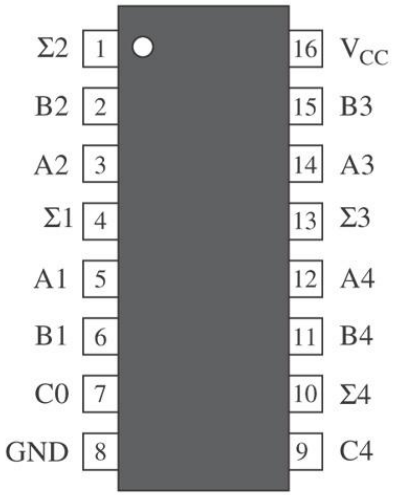


(a) Block diagram

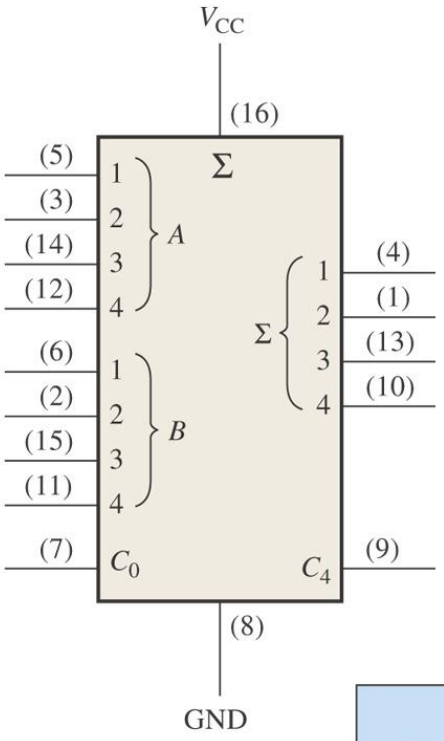


(b) Logic symbol

74LS283 4-bit parallel adder



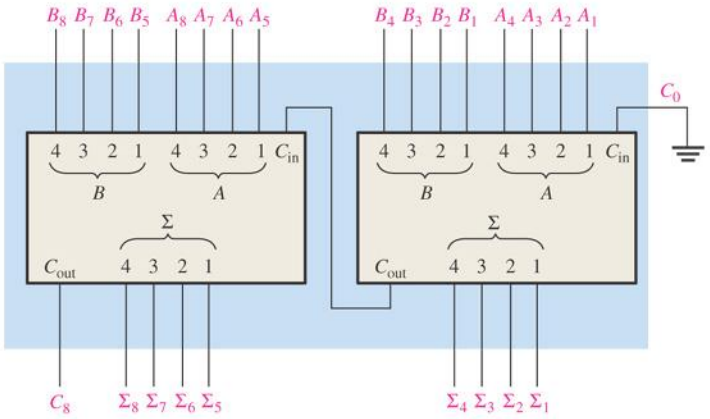
(a) Pin diagram of 74LS283



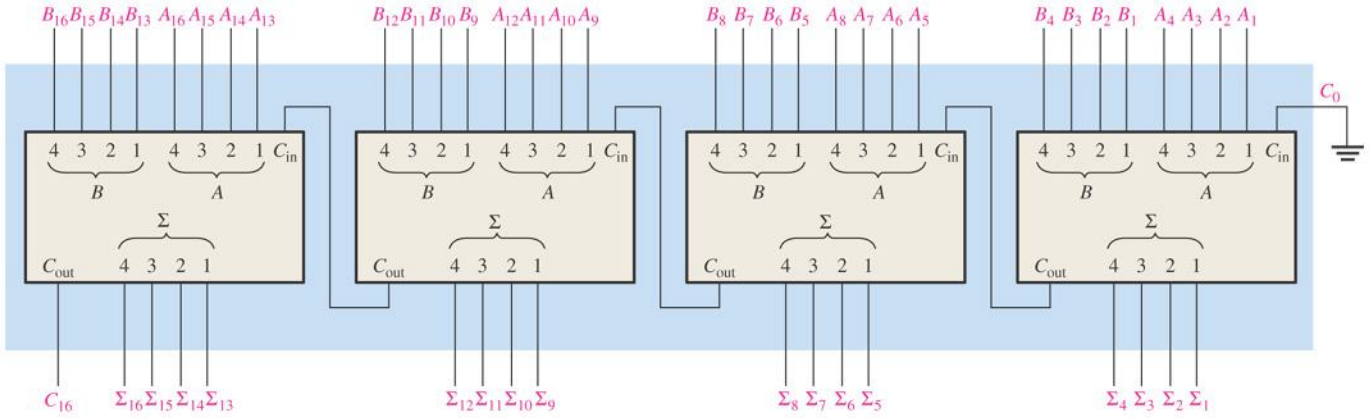
(b) 74LS283 logic symbol

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
t_{PLH} t_{PHL}	Propagation delay, C_0 input to any Σ output		16 15	24 24	ns
t_{PLH} t_{PHL}	Propagation delay, any A or B input to Σ outputs		15 15	24 24	ns
t_{PLH} t_{PHL}	Propagation delay, C_0 input to C_4 output		11 11	17 22	ns
t_{PLH} t_{PHL}	Propagation delay, any A or B input to C_4 output		11 12	17 17	ns

Adder expansion



(a) Cascading of two 4-bit adders to form an 8-bit adder



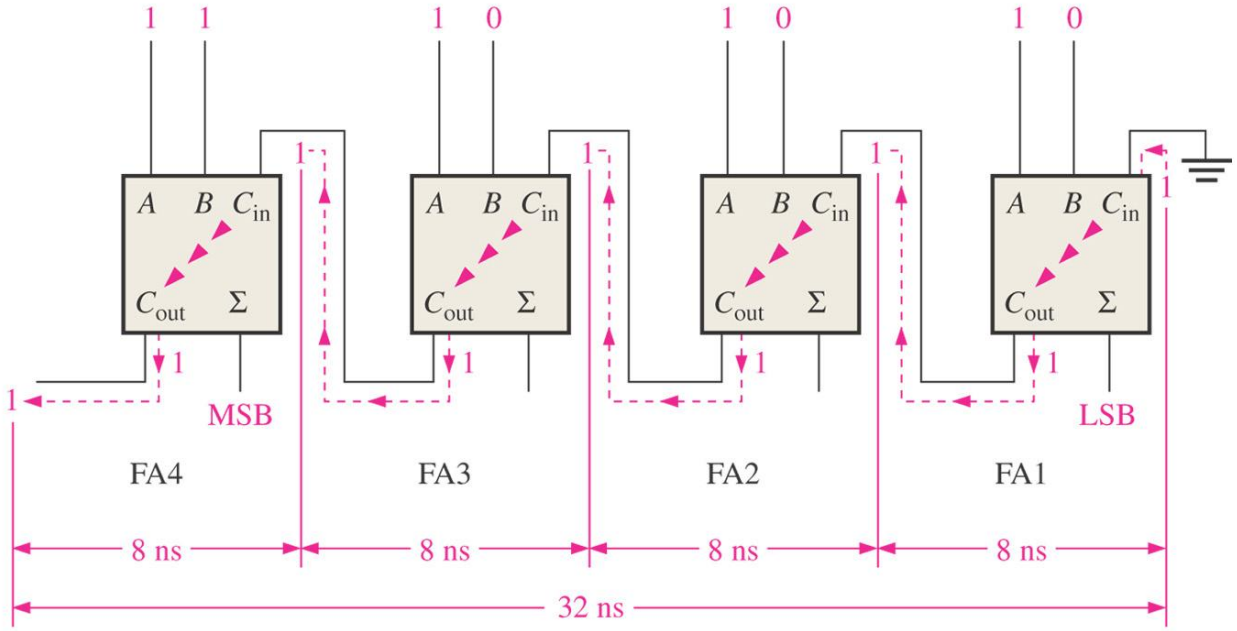
(b) Cascading of four 4-bit adders to form a 16-bit adder

6-3 Ripple Carry Versus Look-Ahead Carry Adders

- There are two categories for parallel adders:
  - Ripple carry
  - Look-ahead carry
- These two categories are fixed by evaluating how *each internal carries are handled from stage to stage*
- The difference – speed of adding numbers
  - Look-ahead carry adder is much faster than ripple carry adder

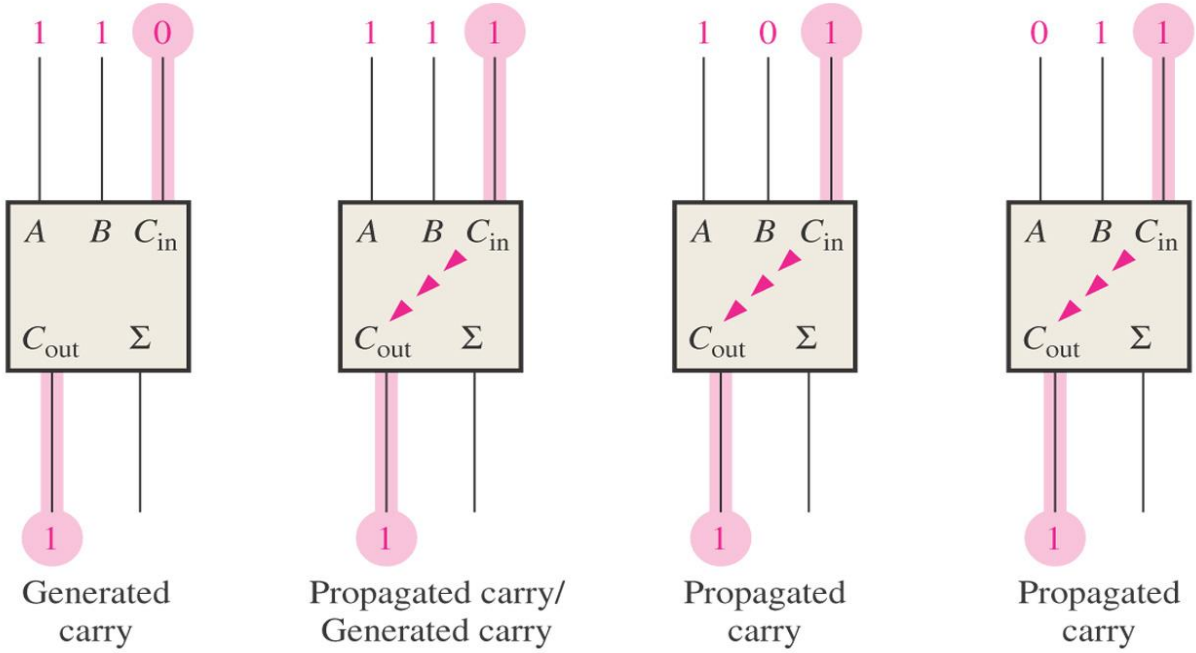
Ripple carry adder

- A ripple carry adder is one in which the carry output of each full-adder is connected to the carry input of the next higher-order stage
- Why delayed/slow?
  - The sum and the output carry of any stage cannot be produced until the input carry occurs



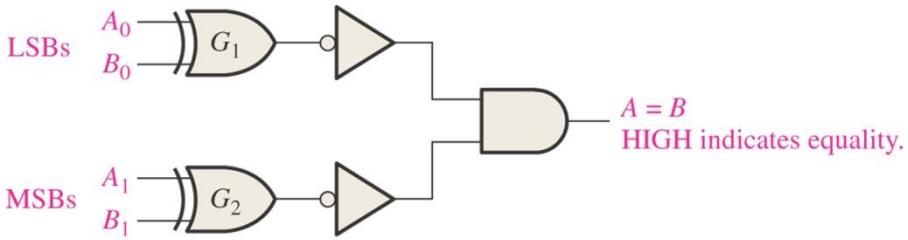
Look-ahead carry adder

- The look-ahead carry adder anticipates the output carry of each stage, and based on the inputs, produces the output carry by either carry generation or carry propagation



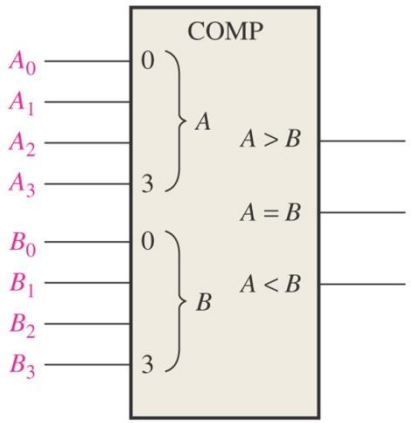
6-4 Comparators

- The function is to compare the magnitudes of two binary quantities to determine the relationship of those quantities
  - Equality

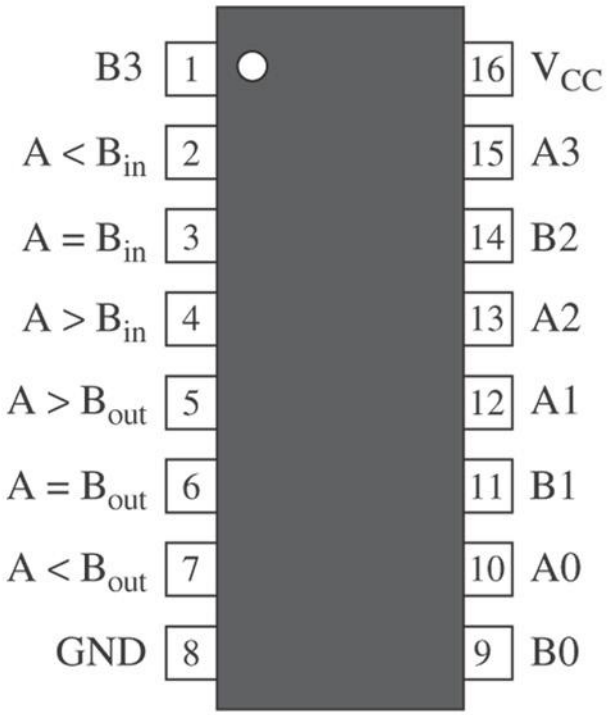


General format: Binary number $A \rightarrow A_1A_0$
Binary number $B \rightarrow B_1B_0$

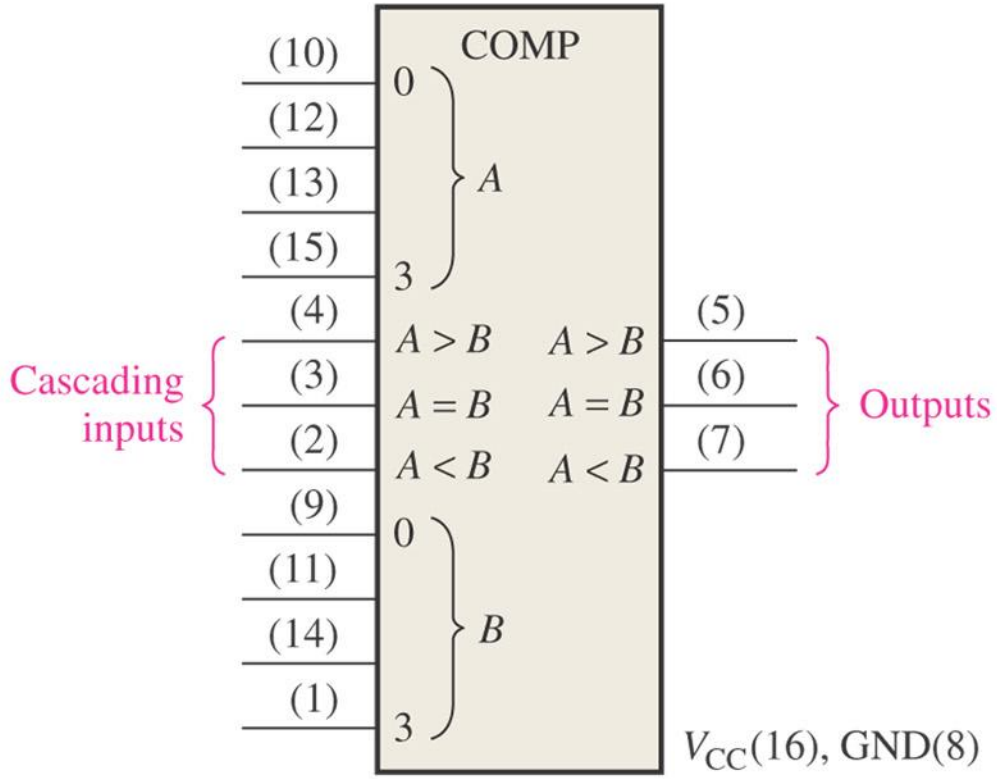
  - Inequality



A 4-bit Comparator (74HC85)

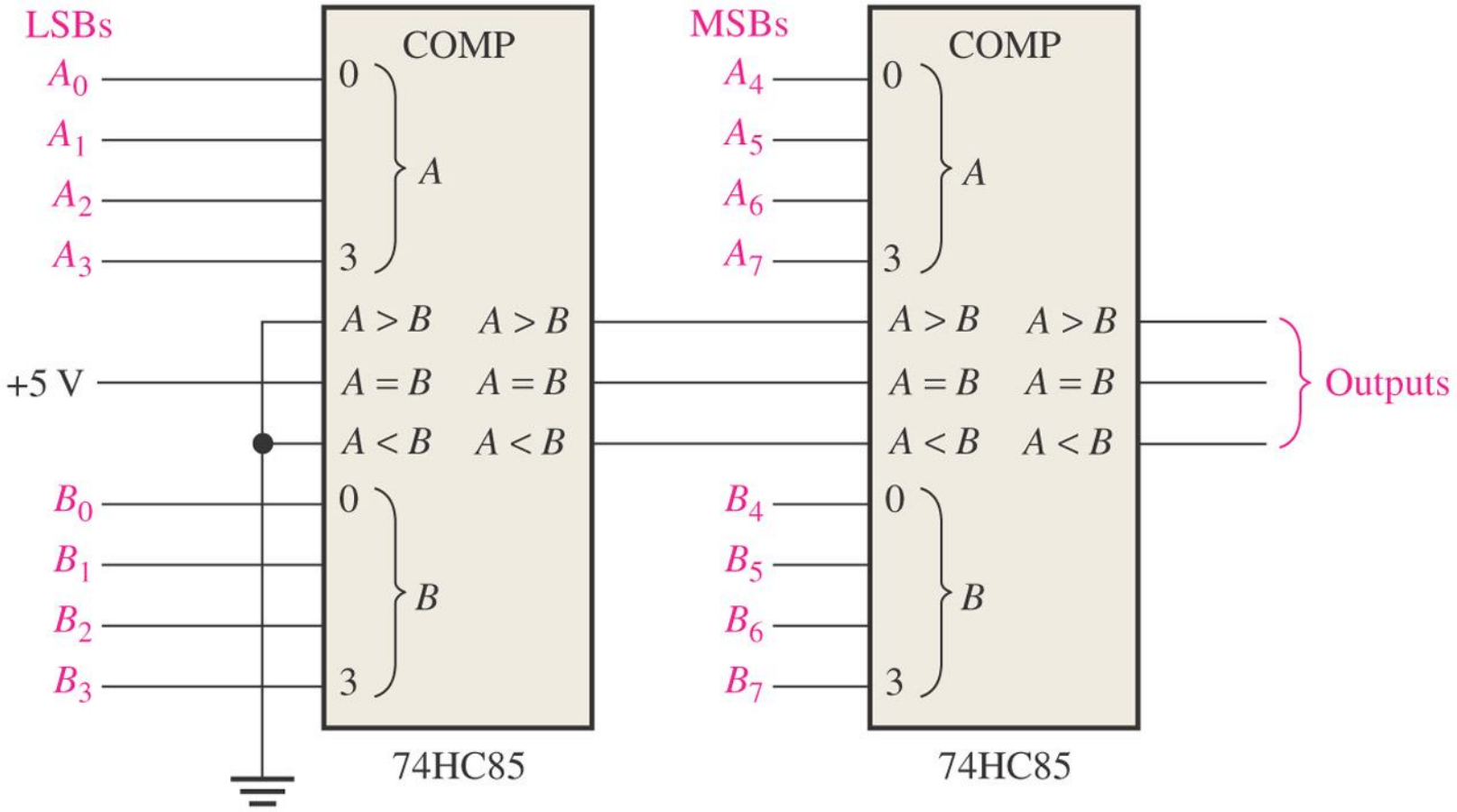


(a) Pin diagram



(b) Logic symbol

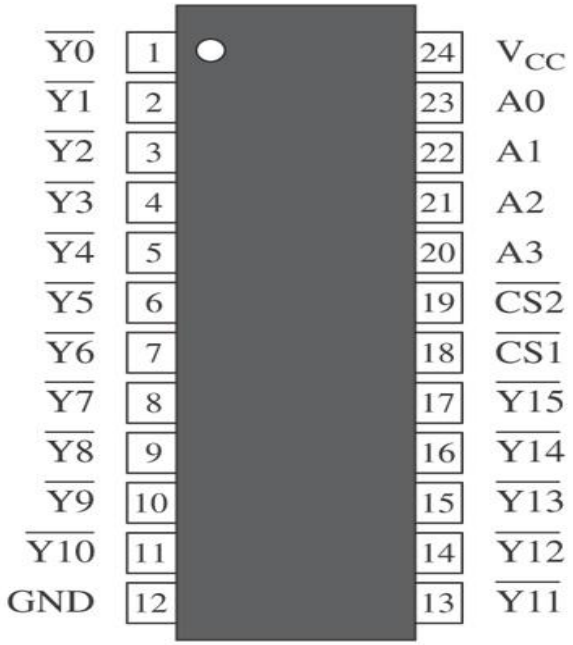
How to connect two 74HS85s



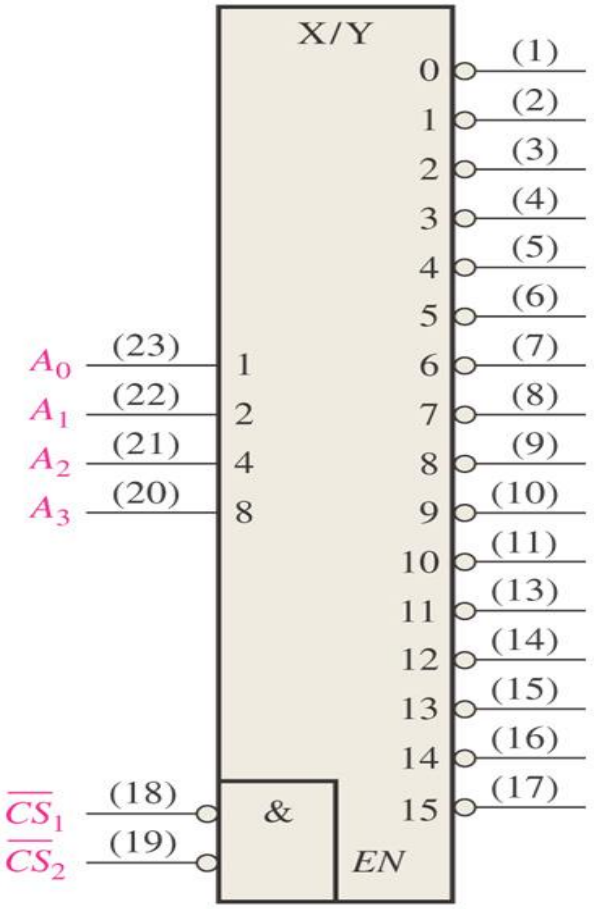
6-5 Decoders

- A decoder is a digital circuit that detects the presence of a specified combination of bits (code) on its inputs and indicates the presence of that code by a specified output level
- Tips to remember when to use decoders:
  - Code (BCD, etc.) → Decimal numbers, etc.

A 1-of-16 Decoder (74HC154)



(a) Pin diagram

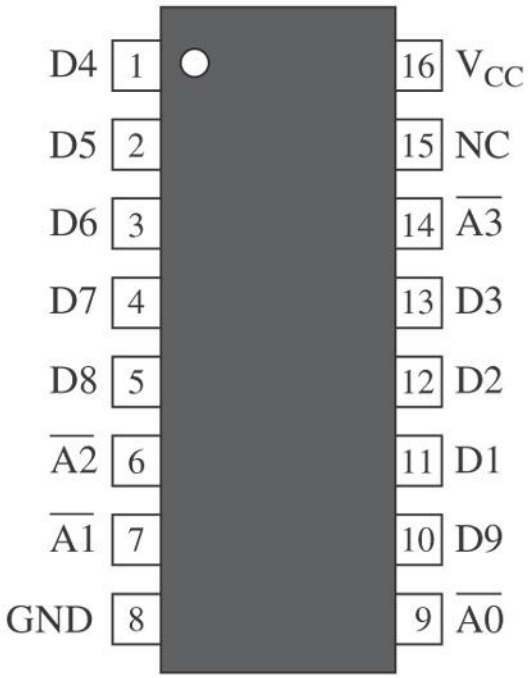


(b) Logic symbol

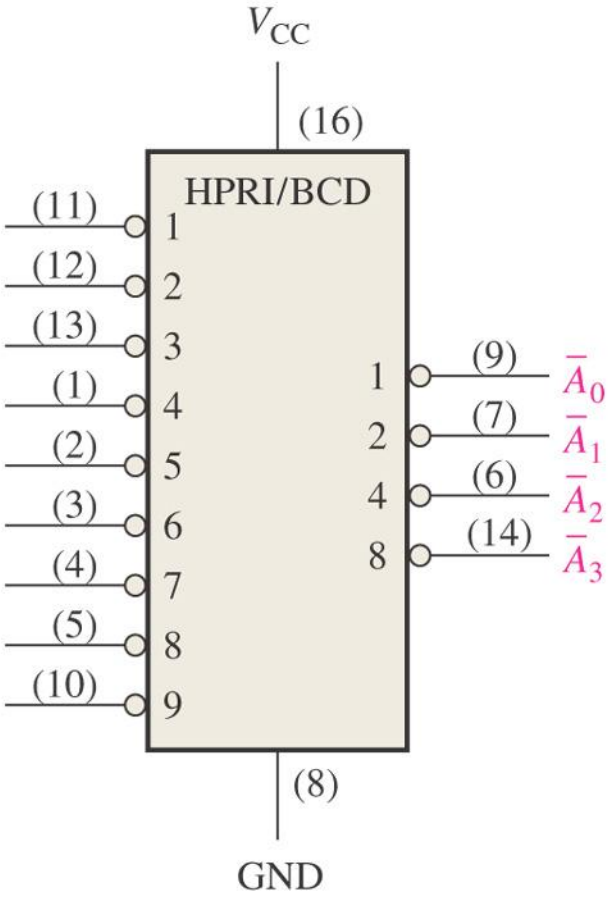
6-6 Encoders

- An encoder is a combinational logic circuit that essentially performs a “reverse” decoder function
- Tips to remember when to use encoders
  - Decimal/octal → BCD or binary

A Decimal-to-BCD Encoder (74HC147)



(a) Pin diagram

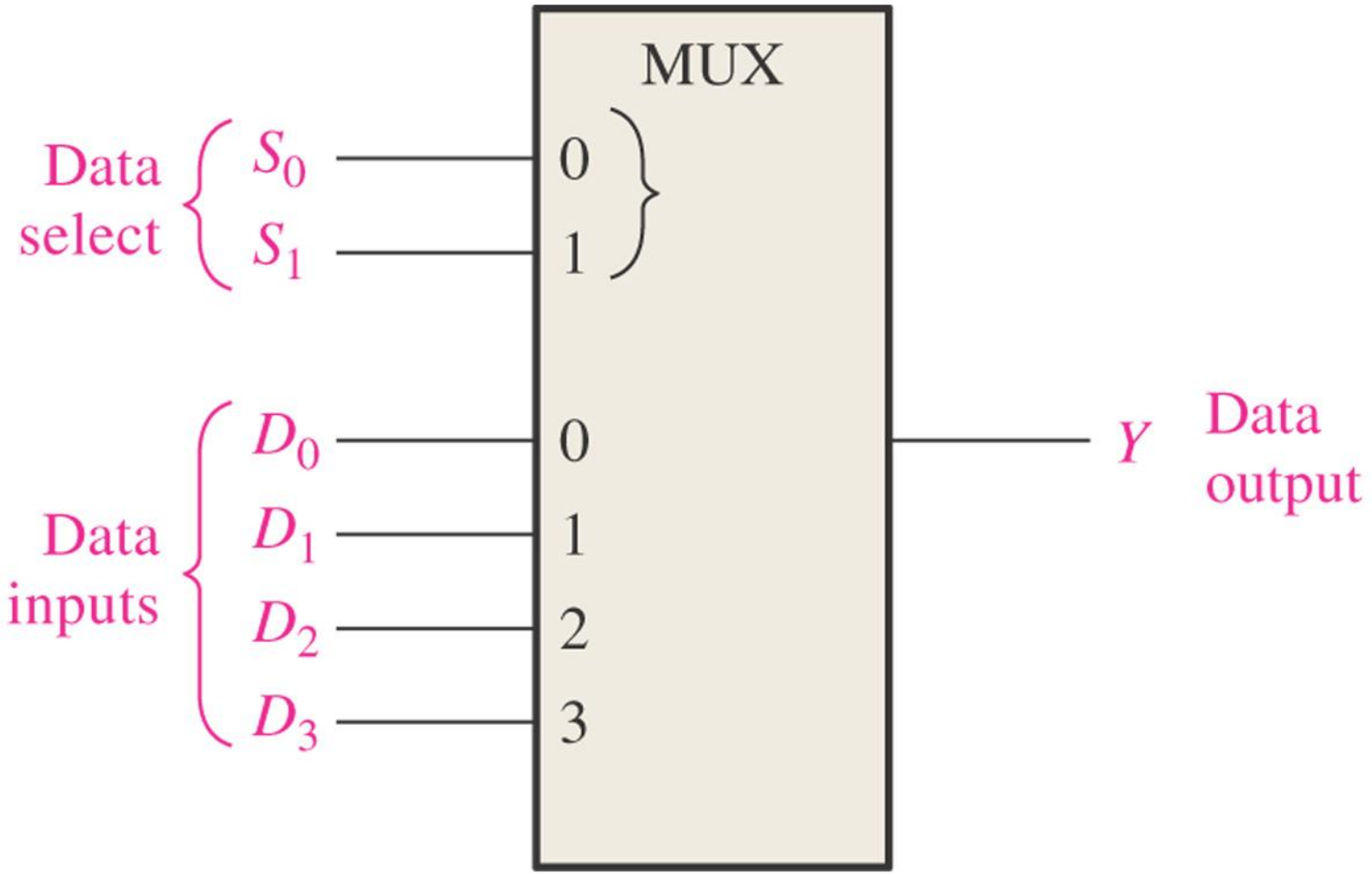


(b) Logic diagram

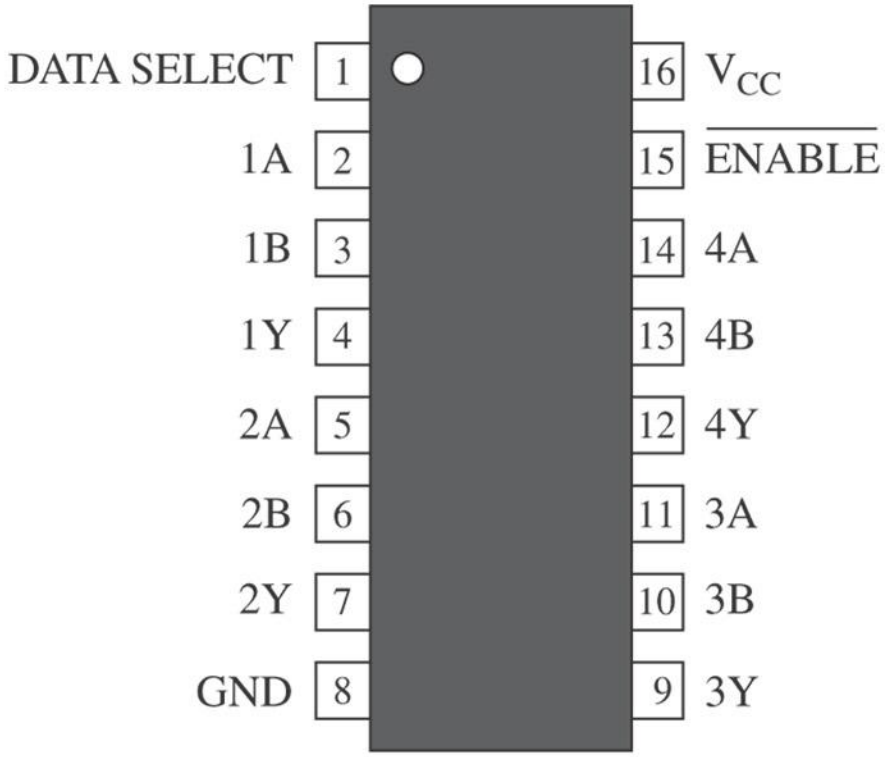
6-8 Multiplexers

- A multiplexer (MUX) is a device that allows digital information from several sources to be routed onto a single line for transmission over that line to a common destination
- Also known as “data selector”

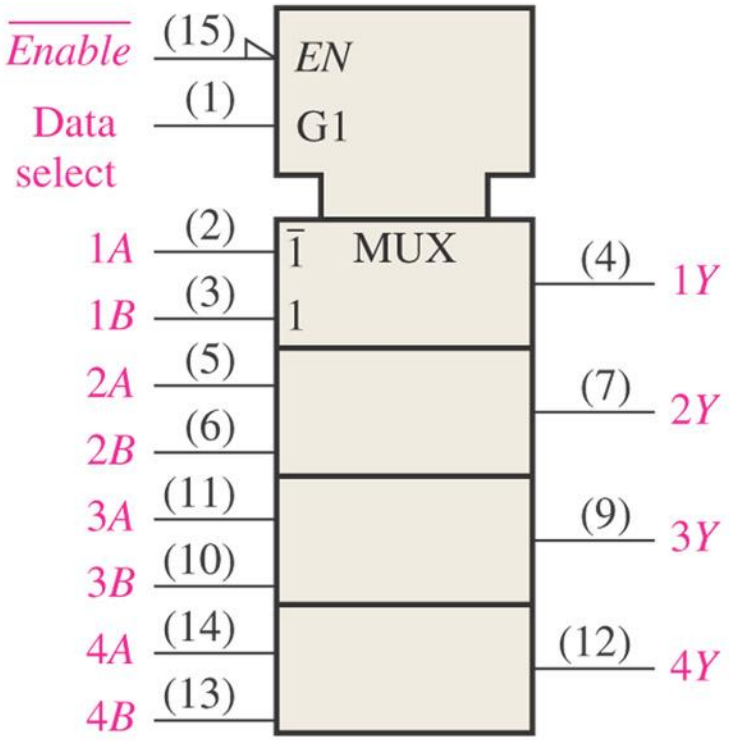
A1-of-4 data selector/multiplexer ()



A quadruple 2-input data selector/multiplexer (74HC157)



(a) Pin diagram

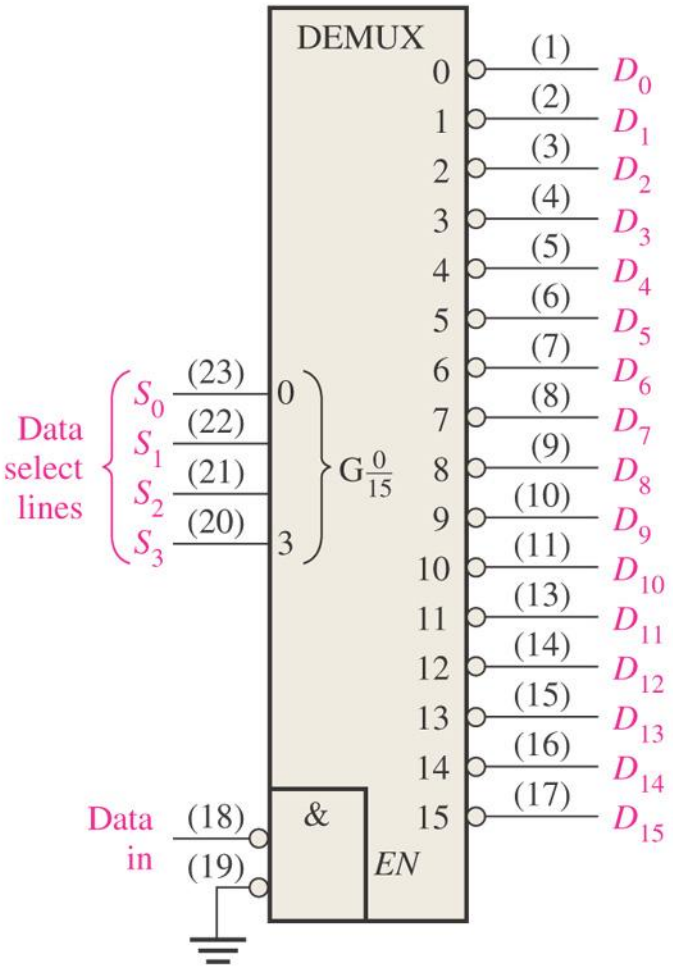


(b) Logic symbol

6-9 Demultiplexers

- In contrast to Multiplexers, demultiplexers (DEMUX) is a device used to distribute a digital information from one line to multiple number of output lines
- Also known as “data distributor”

The 74HC154 decoder used as a demultiplexer



6-10 Parity Generators/Checkers

- Used to check errors while digital codes are transferred from one point to another within a digital system
- Please check previous lecture notes for more details on how parity is checked

Wish you all…
ALL THE BEST IN YOUR FINAL EXAM!!!

Thank you.